



BLAZAR BE2-RMW Accelerator Engine Intelligent In Memory Computing



PRODUCT BRIEF

BANDWIDTH ENGINE (BE) INTRODUCTION

The **BLAZAR Family of Accelerator Engines** support high bandwidth, fast random memory access rates and *embedded In Memory Functions (IMF)* that solve critical memory access challenges for memory bottlenecked applications like network search, statistics, buffering, security, firewall, 8k video, anomaly detect, genomics, ML random forest of trees, graph/tree/list walking, traffic monitoring.

The **Bandwidth Engine 2 (BE2-RMW)** combines the high speed serial memory with the *in memory Bandwidth functions* of the BE2-BURST (but increased the number of functions) and now adds *in memory Compute functions* called RMW. RMW functions are a family of functions that modify memory locations utilizing an ALU to perform Read/Modify/Write operations.

Applications benefits...

- FPGA Acceleration for Xilinx and Intel
- Replaces up to 4 QDR/RLDRAM memory devices
- Memory architecture allows up to 32 simultaneous accesses
- Lowers latency up to 4x and increases available access rates 6x by avoiding memory bottlenecks
- **Accelerates FPGA application by providing fast, efficient, single function for**
 - **Enhanced Burst Functions (Reference BE2-Burst)**
 - **Powerful RMW Functions.**
 - **Total of over 50 IMFs on this device.**
- The devices support application acceleration for aggregate throughput rates ranging from 70Gb/s to over 360Gb/s per device
- Facilitates a "Software Define-Hardware Acceleration" system architecture

KEY FEATURES / PRODUCT OPTIONS

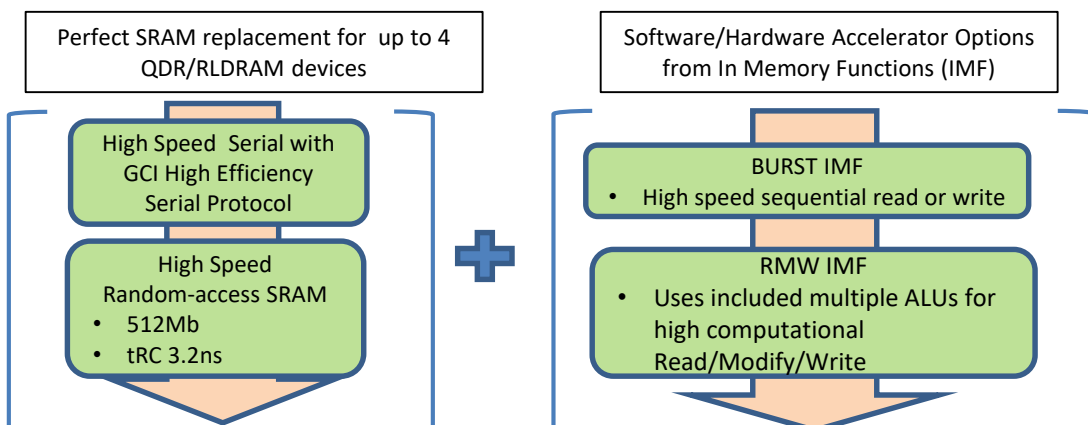
- High Bandwidth, low pin count serial interface
 - Highly efficient reliable transport command and data protocol optimized for 90% efficiency
 - Eases board layout and signal integrity, no trace length matching required, operates over connectors
- 512Mb SRAM (8M x 72b)
- High access rate SRAM class memory
 - Up to 3.3 Billion transactions/sec
- High cycle rate memory
 - 3.2ns tRC
- Latency: 16ns external (pin to pin)
- **In Memory Bandwidth Functions**
 - BURST *sequential read and write* functions for *Data Movement* nearly doubles bandwidth
 - Burst length: 1, 2, 4, 8 x 72b
 - Reduction of I/O up to 7X
- **In Memory Compute Functions**
 - Applications focused *Read/Modify/Write* operations for *Data Modification* that execute by issuing a single command, saving the typical 3 operations normally required
- Highest Single Chip Bandwidth – up to 320 Gbps throughput

APPLICATIONS FOCUS

- High bandwidth random/sequential data access/movement applications
- Statistics, Metering, security, buffering
- Applications needed large SRAMs.
- FPGA Acceleration for Xilinx and Intel

MoSys ACCELERATOR ENGINE Elements

MoSys Engines have a Unique Memory Architecture that can replace SRAM/RLDRAM memories and embeds In Memory Functions (IMF) that execute many times faster. A single embedded function can replace several traditional memory accesses.





MoSys Bandwidth Engine RMW (BE2) Architecture



Fixed In Memory COMPUTE Functions-RMW (In addition to the BURST functions IMFs)

The RMW Functions are focused on accelerating atomic DATA MODIFICATION where coherent updates are needed by reducing the I/O overhead and insuring correct results with a short ECC protected pipeline utilizing data forwarding.

Provides an alternative to a long pipeline which sends one command to READ a memory location, a second operation to MODIFY the value, and a third command to WRITE the new value back to the memory location.

Saves time not having to move data in/out of memory and external modification time. RMWs are atomic, thus ensuring correct multi-threaded behavior.

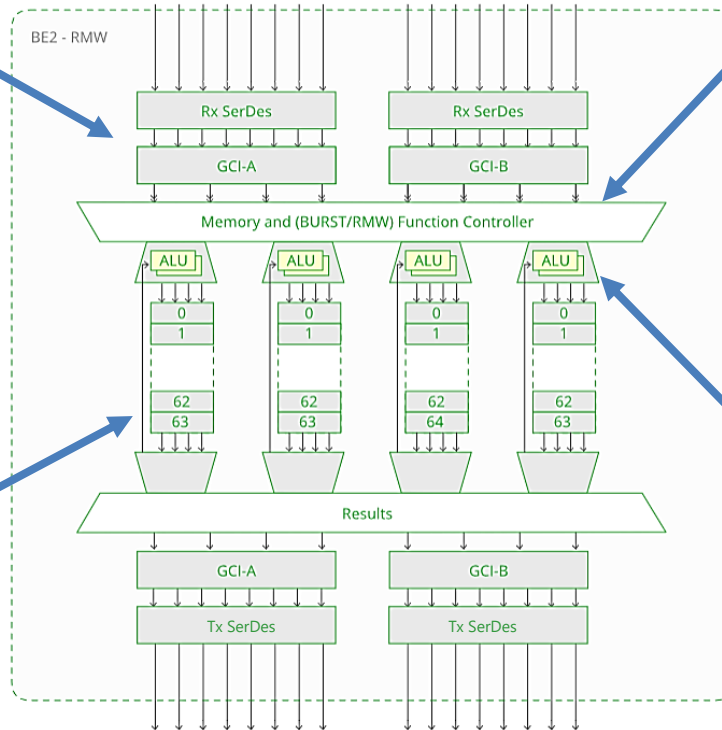
I/O reduction up to 7X and avoids stale data problems.

High speed serial I/O

- GCI serial I/O versions of 10, 12.5 Gbps for high bandwidth (up to 320 Gbps)
- Device can operate with a minimum of 4 lanes.
- Has two, full duplex 8 lane ports that operate independently
- Reduces number of signal pins over traditional memories, increases signal integrity allowing longer board traces to ease board signal routing
- Operates across connectors

Main Memory

- 512Mb (BE3 has 1Gb)
 - 4 partitions/64 banks
 - 8 READ & 8 WRITE ports
- 3.2 ns tRC
- Allows parallel partition & Bank execution



Memory/Function Controller

- Resolves localized bank conflicts
- Directs read/write function execution to selected bank of memory
- Manages the sequence of operations to execute
 - BURST – Sequential read or writes
 - RMW -- 4-8x reduction in RMW accesses
- Controls parallel function execution

ALU

- Embedded RMW Functions utilize ALUs for in memory computational functions
 - There are 8 ALUs (BE3 has 16)
 - Simultaneous operations

Software Define - Hardware Accelerated

www.mosys.com LEARN MORE:
<https://mosys.com/blazar-family-of-accelerator-engines/>

SOFTWARE DEFINED...HARDWARE ACCELERATED

Software and System Architects can improve application performance by accelerating the memory access and utilizing the In Memory Compute Functions.

The different Accelerator Engine devices allow application tuning to achieve increasing levels of performance up to our most powerful engine... the Programmable HyperSpeed Engine with 32 Processor Cores.

	Part Number	Description	Package	Interface			Memory		Access Rate		Commands /Functions			
			Pkg Size mm	Lanes Tx/Rx	Rate per Lane 10-12.5G 15G 25-28G	BW Gb	tRC ns	Size Gb	Billion Transaction/s	R/W	RMW / ALU	Custom 32 RISC Cores		
BURST	MSR620	Bandwidth Engine 2 Burst Serial 0.5Gb High Access Memory	FCBGA 19x19	16	✓			320	3.2	0.5	3.3	✓		
	MSR630	Bandwidth Engine 3 Burst Serial 1Gb High Access Memory	FCBGA 27x27	16	✓	✓	✓	717	2.7	1	6.5	✓		
RMW	MSR820	Bandwidth Engine 2 RMW Serial 0.5Gb High Access Memory with ALU for RMW functions	FCBGA 19x19	16	✓			320	3.2	0.5	3.3	✓	✓	
	MSR830	Bandwidth Engine 3 RMW Serial 1Gb High Access Memory with ALU for RMW functions	FCBGA 27x27	16	✓	✓	✓	717	2.7	1	6.5	✓	✓	
Program	MSPS30	Programmable Accelerator Engine Serial Interface, 1Gb Memory, 32 RISC Processor cores for custom algorithms, compute, functions	FCBGA 27x27	16	✓	✓	✓	717	2.7	1	24 Internal	✓	✓	✓

