MSPS30 – Programmable Search Engine

PRODUCT BRIEF

MSPS30 DESCRIPTION

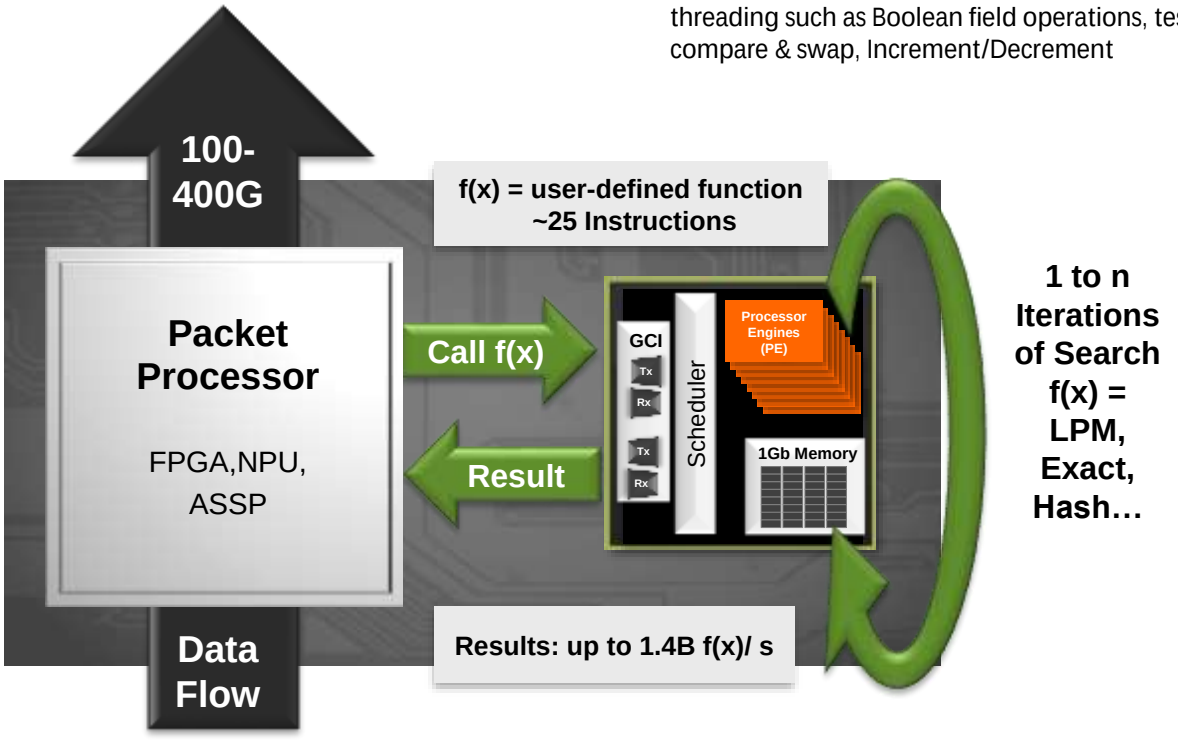
The MSPS30 (PSE-S30) is a monolithic IC leveraging MoSys® Programmable Search Engine (PSE) architecture. The device features a pin efficient high speed serial interface where the host device can access up to 32 search optimized processor engines running user-defined functions. The processors access up to 1Gb of high speed table memory using single or atomic RMW operations and return the results to the host through the serial interface. High internal throughput, efficient schedulers supporting up to 8 domains provide coherency and performance. The PSE-S30 device can implement high speed search, compute or other custom functions to accelerate networking, security, test, video, monitoring, data center smart NIC cards and other applications benefiting from the performance benefits of in-memory algorithm acceleration and/or compute.

PROGRAMMABLE SEARCH ENGINE

The Programmable Search Engine (PSE) architecture features 32 search-optimized processor engines, data flow schedulers, and over a terabit of internal access bandwidth. The device leverages MoSys' proven serial GigaChip® Interface technology and high density integrated memory (1152 Mb of 1T-SRAM® embedded memory). The 32 processor engines have direct access to integrated table memory through an internal interconnect and scheduler architecture.

KEY FEATURES

- **High-speed serial interface and protocol**
  - Up to 800Gbps interface throughput (up to 28G/lane)
  - Interface scales from 4 to 16 lanes to optimize bandwidth and pin count
  - Independent access from two host devices
  - PHY complies with IEEE and OIF standards
  - Up to 1.4B/s user defined commands with 8 lanes
- **32 multi-threaded 1.5GHz processor elements**
  - Load and store processor architecture
  - Instruction enhancements for packed data structure access such as hashing, field extract/insert, multi-field compare, multi-way branch, sparse matrix compression, bit string and command parsing
  - 8 Threads per processor engine for maximum utilization
  - User-defined short micro-coded search functions called through interface commands. Examples of types that can be built are exact, wildcard, longest prefix, string match and more called through interface commands
- **Integrated interconnect, scheduler, and 1Gb of table memory for internal multi-cycle performance**
  - Over 1.5Tbps internal bandwidth, 2x the interface rate
  - Over 5B reads and 5B writes per second
  - Eight scheduling domains for performance optimization
  - Supports direct R/W or RMW memory access
  - Built-in atomic memory operators in support of multi-threading such as Boolean field operations, test & set, compare & swap, Increment/Decrement



USER-DEFINED FUNCTIONS

The 32 processor engines on the PSE-S30 device are organized as eight clusters of four processor engines. Each processor engine can support 8 threads that can access the scheduler and table memory. The host device issues commands that call single or multi-iteration functions such as hash, exact match, longest prefix match, etc. Commands can be issued at rates up to 1.4B/s typically over 8 serial lanes. The functions or subroutines are typically comprised of roughly 20-25 instructions and 3 to 4 reads/writes. Users can leverage internal IP to create custom functions using the IDE tool and PSE-S30 model or request MoSys and/or our partners to develop specific application code and software interface.

DEVELOPMENT TOOLS

- Integrated Development Environment (IDE) for custom code development
- Proven FPGA & ASIC host controller
- PSE-S30 models
- Evaluation platforms with FMC connectors
- Advanced debugging and evaluation capabilities with MoSys IC Spotlight™ Analyzer software

GIGACHIP INTERFACE

GigaChip Interface (GCI) is an open, freely licensable, efficient transport layer built on compatible, industry standard SerDes. GCI is optimized for small packet, chip-to-chip communications including error detection and recovery mechanisms.

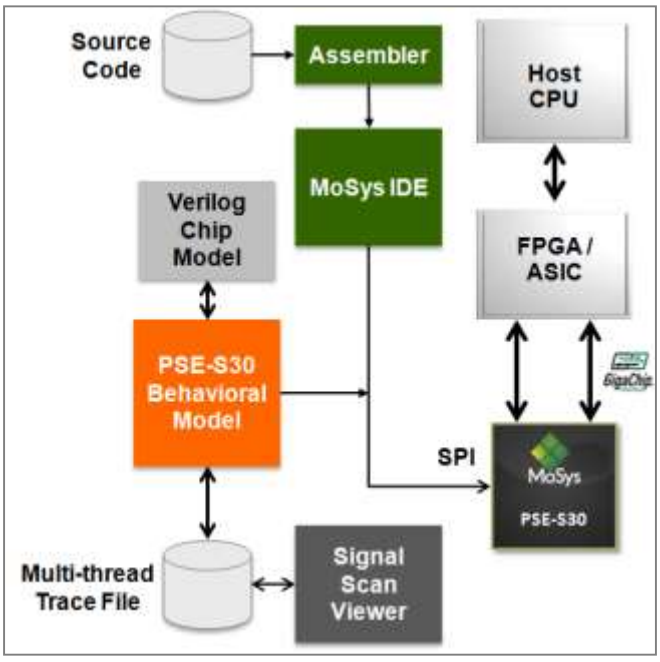
GIGACHIP FRAME FORMAT

The GigaChip Interface uses a fixed-size 80-bit frame, consisting of 72-bit payload, 6 bits of CRC and 2 control bits, providing 90% transport efficiency. Each lane is scrambled with a pseudo-random bit sequence, providing sufficient transition density and DC balance for reliable, high-speed serial communications without the overhead of 8b/10b encoding.

PSE TRANSACTION LAYER

The PSE transaction layer fits within the GigaChip Interface frame format and calls the custom Subroutines (CSUB) functions from the host and returns the results from the PSE-S30.

INTEGRATED DEVELOPMENT ENVIRONMENT FLOW



BOARD DESIGN ATTRIBUTES

- 676 FCBGA, 27mm x 27mm, 1.0mm ball pitch
- 0.9V/1.0V, 1.5V, (1.8V EEPROM) supplies
- IEEE 1149.1/1149.6 JTAG boundary scan
- SPI / I2C configuration port

ORDERING INFORMATION

Base Part Number	Temperature	Speed
MSPS30AAC-12	C	-25
	E	-15

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