LineSpeed™ Flex MSH321

100G Multi-Link Gearbox for Modules

PRODUCT BRIEF

MSH321 DEVICE OVERVIEW

The MoSys® LineSpeed Flex 100G Multi-Link Gearbox (MLG) is a single chip CMOS device that enables high-density, independent 10GE and 40GE interfaces to be multiplexed into a single 100GE interface.

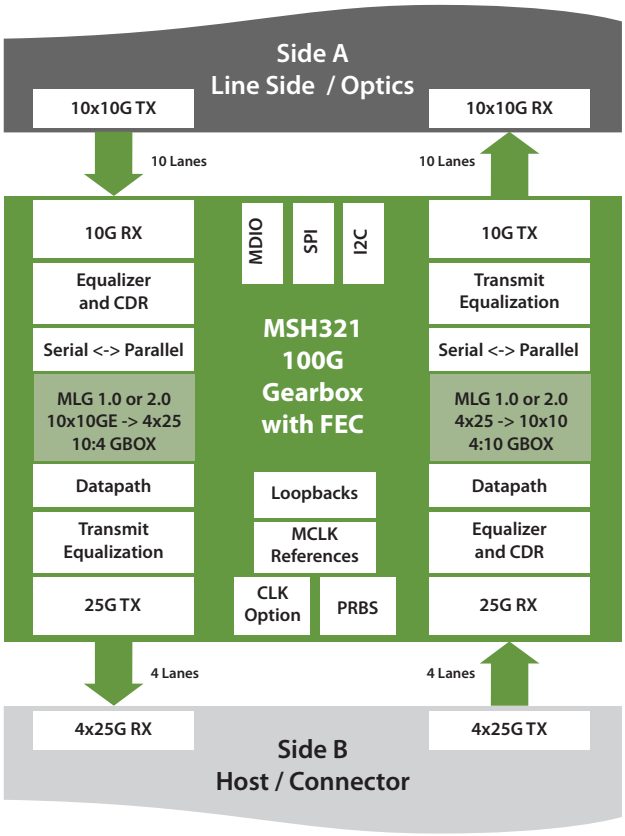
The device supports both OIF MLG-1.0 and MLG-2.0 standards that aggregate a combination of 10GE and 40GE links, up to 100G total bandwidth, and converts that to a single 100GE (4x25G) link. As physical interfaces on switching and packet processing ICs move to 25G PHY interfaces for performance and board density, the MLG function allows large scale systems built supporting the MLG protocol to support higher port counts of 10GE and 40GE interfaces.

MSH321 DEVICE DESCRIPTION

The MSH321 100G MLG Gearbox device performs all alignment marker insertion and awareness, idle insertion and deletion, and data alignment required by the OIF MLG standards. The MSH321 also has optional support for the IEEE802.3ba standard gearbox function. The electrical interfaces support IEEE and OIF-CEI-3.0 10G and 25/28G specifications.

Configuration of the device is supported through an I2C, MDIO or SPI interface.

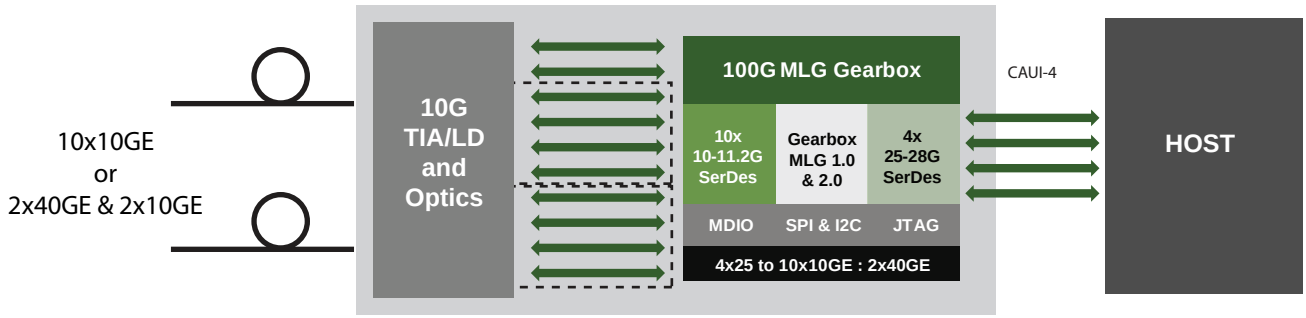
The device supports extensive test and monitor functions including PRBS Generators and checkers, error and eye quality monitors, alarms, and MLG link monitor registers.



FEATURES

- Supports OIF MLG 1.0 and MLG 2.0 Standards
  - 10 Independent 10GE links into 100GE (4x25G)
  - Mix of 10GE and 40GE links into 100GE (4x25G)
- Optional for IEEE 802.3ba Gearbox for Ethernet & OTN
- IEEE and OIF 10, 40 and 100G electrical standards
- Self adapting equalizer - eye opening capability
- Integrated Rx 100 ohm termination resistors and AC coupling
- Flexible power and configuration options
- Transmitter and TX pre-emphasis
- Per lane PRBS generator and bit error rate checker
- Reverse polarity control on all inputs and outputs
- Monitor and reference clock support
- Internal registers can be accessed by I2C, MDIO or SPI ports
- Base register configuration and FW provided for ease of use
- Small 12x12mm FCCSP package support module applications

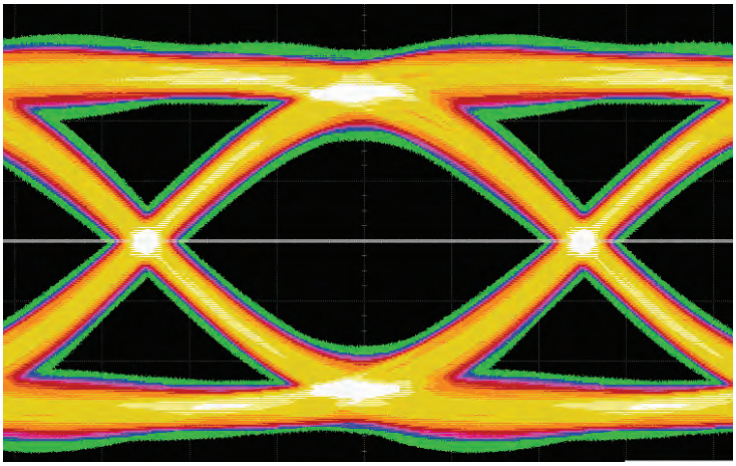
MSH321 APPLICATION EXAMPLE



MSH321 DEVICE SIGNAL INTEGRITY

To ensure signal integrity for 10G and 25G interfaces, the MSH321 has the following circuits:

- Opening the eye: A combined analog and digital RX Equalizer
- Retiming: A data slicer plus a clock and data recovery circuit
- Bit stream alignment: Deserializer, frame sync and deskew functions
- Clock synchronization: An elastic buffer for data alignment
- Pre-distortion compensation: A serializer and transmit equalization circuit



PACKAGING

- 12mm x 12mm FCCSP (0.5mm)
- Pin Compatible with LineSpeed Flex 12mm Devices

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