MSR830 - Bandwidth Engine® 3 – Macro

Fast, Intelligent Data Access

PRODUCT BRIEF

MSR830 DESCRIPTION

The MoSys® MSR830 is a member of the Bandwidth Engine 3 serial memory family with 16 lanes of full duplex SerDes running up to 25Gb/lane, 1152 Mb of 1T-SRAM® memory and integrated access scheduling. It can perform atomic operations for metering, single-counter and dual-counter updates for statistics and policing as well as other applications. The SerDes interface delivers full duplex, CRC protected data throughput and over ten billion memory transactions per second.

BANDWIDTH ENGINE OVERVIEW

The Bandwidth Engine architecture is a highly parallel, multi-bank, multi-ported 1T-SRAM based memory array coupled with a high efficiency serial interface and on-board functionality, delivering intelligent scheduled access in addition to the highest memory transaction rate, table read rate and data throughput of any single chip device.

APPLICATIONS

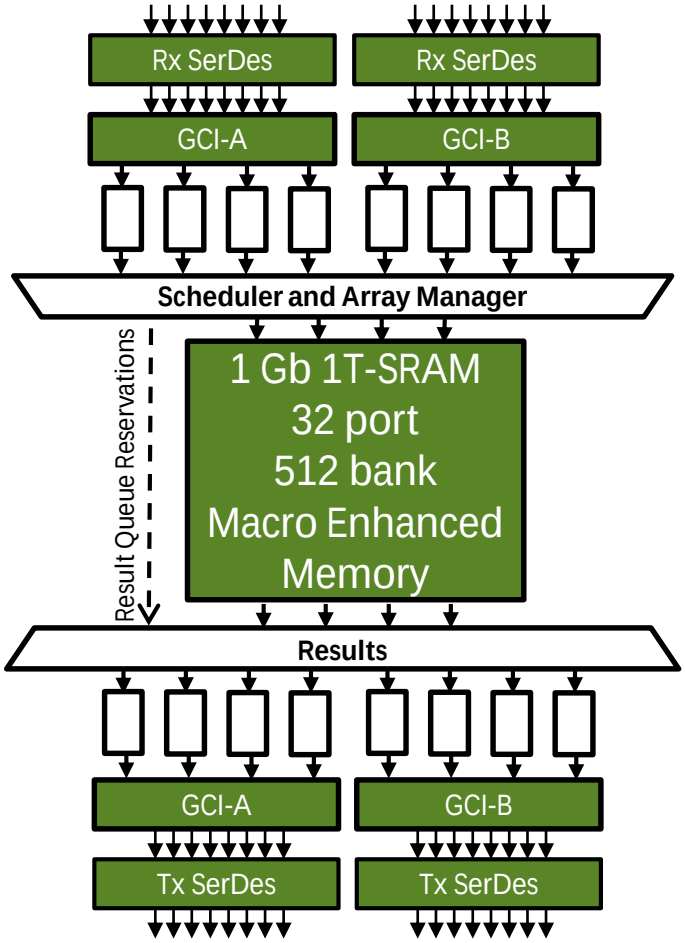
The MSR830 is commonly used for line rate statistics and metering and can also perform buffering, table lookup or a combination thereof in a unified memory application. A single MSR830 is capable of supporting these multiple applications and can also be shared between two host devices; each connecting to one GCI port. For greater capacity (up to 4.5Gb of total memory capacity), the narrower lane configurations allow multiple MSR830 devices to be connected using the 16 SerDes on the host device.

At the board level the MSR830 can achieve smaller board area, easier routing, lower power consumption and a superior economic solution.

PERFORMANCE

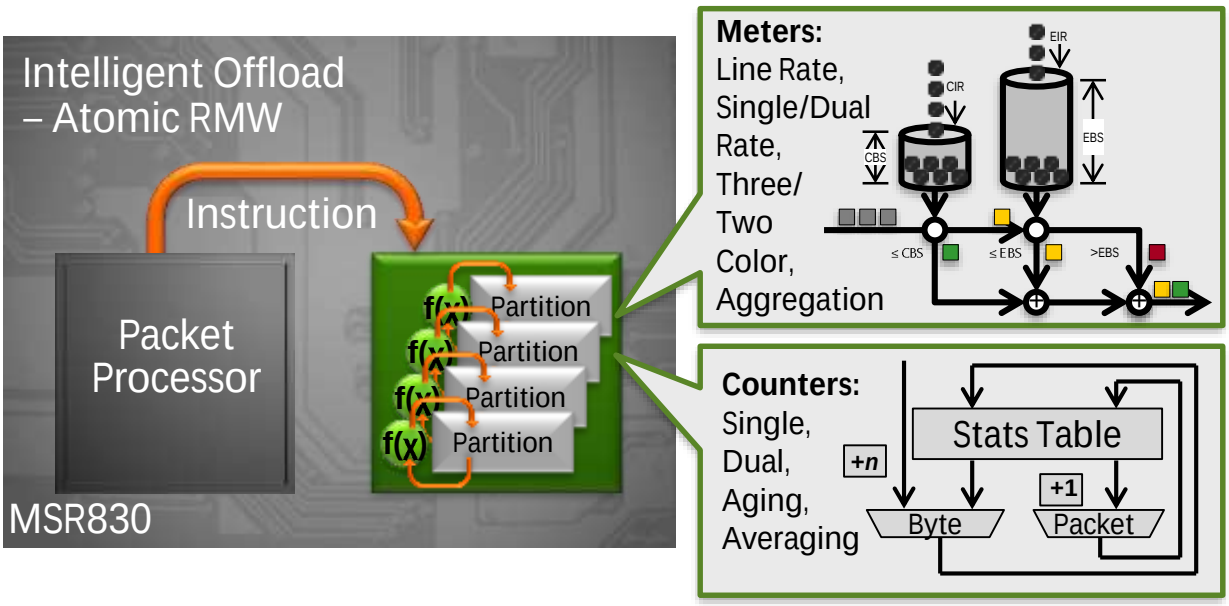
The metering and counting functions of the MSR830 Bandwidth Engine 3 - Macro device can be used for Shaping or Traffic Conditioning in traditional enterprise, metro and carrier class services. A single device can support dozens of 100G ports with a single counter pair or can support many counters per port or higher port rates when they become available.

In addition, datacenter and emerging high rate Software Defined Network (SDN) and Network Function Virtualization (NFV) can also take advantage of the offload statistics acceleration and high access rate for table lookups for flow based and application aware switching and routing.



FEATURES

- 1152Mb 1T-SRAM® memory array architecture
  - 3.2 ns core cycle time
- Low-latency SerDes technology
  - 4, 8 or 16 serial transceivers (TX/RX)
  - OIF CEI-11G-SR and CEI-28G-VSR compatible
  - Tuned for low-power transmission up to 20 cm
- Open GigaChip® Interface delivers bandwidth, efficiency and reliability
  - Low latency protocol
  - Reliability with scrambling, CRC and error recovery mechanisms
- Intelligent Error Management and Bit Safe® Technology
- High reliability – 1T-SRAM soft error immunity
- Advanced debugging and evaluation capabilities with MoSys IC Spotlight software



BUILT-IN COUNTERS AND METERS

The MSR830 with a single instruction can perform a single or dual counter update, it also includes counter aging and averaging.

The MSR830 supports many common RFC and MEF metering standards and is capable of metering each flow to a unique rate and criteria, including meter credit overflow and coalescence.

UNIFIED MEMORY IMPLEMENTATIONS

The functionality is selectable on a cycle by cycle basis, allowing the use of the device in unified memory applications. Multiple tables, buffers, counters and meters can be defined with access interspersed between applications which could use each access command as needed.

BOARD DESIGN ATTRIBUTES

- 676 FCBGA, 27mm x 27mm, 1.0mm ball pitch
- 0.9V/1.0V, 1.5V, (1.8V EEPROM) supplies
- IEEE 1149.1/1149.6 JTAG boundary scan
- SPI / I2C configuration port

ORDERING INFORMATION

Base Part Number	Temperature	Speed
MSR830AA	C	-25
	E	-15
		-12

GIGACHIP INTERFACE

The GigaChip Interface (GCI) is an open, freely licensable, efficient transport layer built on compatible, industry standard SerDes. GCI is optimized for small packet, chip-to-chip communications including error detection and recovery mechanisms.

GIGACHIP FRAME FORMAT

The GigaChip Interface uses a fixed-size 80-bit frame, consisting of 72-bit payload, 6 bits of CRC and 2 control bits, providing 90% transport efficiency. Each lane is scrambled with a pseudo-random bit sequence, providing sufficient transition density and DC balance for reliable, high-speed serial communications without the overhead of 8b/10b encoding.

MoSys

2309 Bering Drive
San Jose, CA 95131
Tel: 408-418-7500
Fax: 408-418-7501

For more information
www.mosys.com

 PB-608 1218