MSR630 - Bandwidth Engine® 3 – Burst

Fast, Intelligent Data Access

PRODUCT BRIEF

MSR630 DESCRIPTION

The MoSys® MSR630 is a member of the Bandwidth Engine 3 family with 1152 Mb of 1T-SRAM® memory and on-board access scheduling. The SerDes interface delivers full duplex, CRC protected data throughput and over five billion memory reads per second.

BANDWIDTH ENGINE OVERVIEW

The Bandwidth Engine architecture is a highly parallel, multi-bank, multi-ported 1T-SRAM based memory array coupled with a high efficiency serial interface and on-board functionality, delivering intelligent scheduled access in addition to the highest memory transaction rate, table read rate and data throughput of any single chip device.

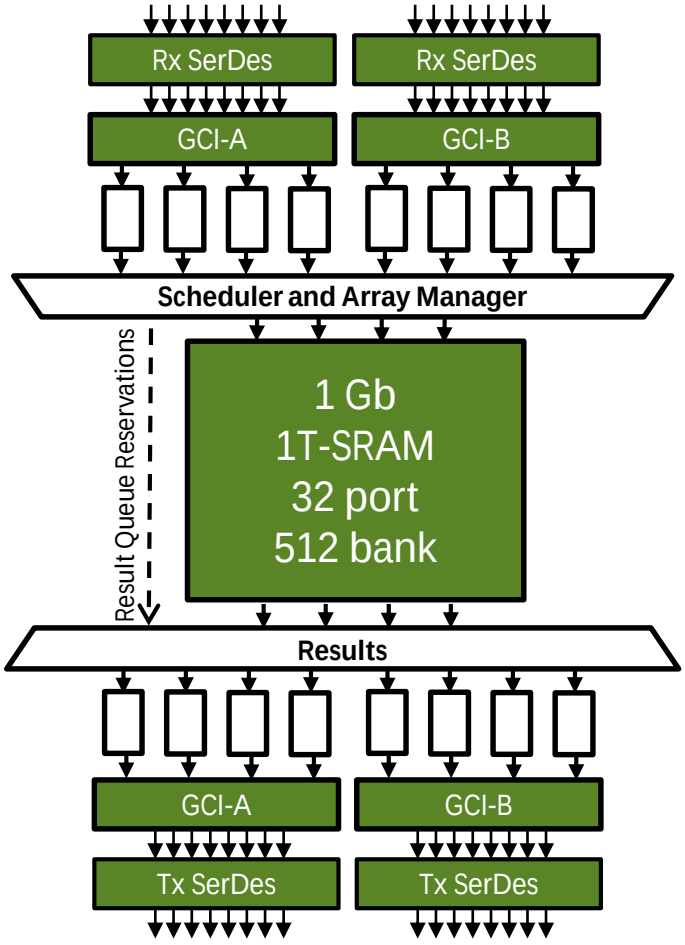
APPLICATIONS

The MSR630 is a high bandwidth and high access serial memory commonly used for high performance buffering, table lookup or a combination thereof in a unified memory application. This performance is useful in a variety of memory intensive applications for networking, embedded, video processing, data processing and high performance compute acceleration markets. raditional memory solutions may require one type of memory for buffer performance and a second type for the high read rate required for table lookup or similar applications. A single MSR630 is capable of supporting these multiple applications and can also be shared between two host devices; each connecting to one GCI port.

At the board level the MSR630 can achieve smaller board area, easier routing, lower power consumption and a superior economic solution.

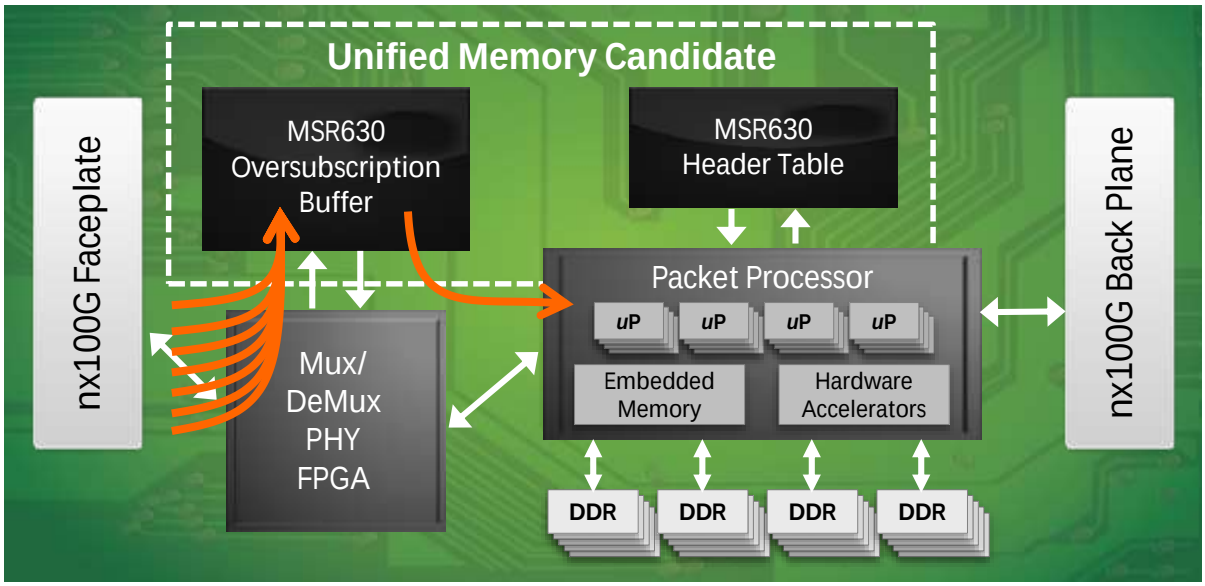
PERFORMANCE

Throughput (Gbps)		Speed Grade		
		-12	-15	-25
Width	Burst	12.5	15.6125G	25G
16 lane	BL8	**160**	**200**	**320**
	BL4	144	180	288
	BL2	**120**	150	240
8 lane	BL8	**80**	**100**	**160**
	BL4	72	90	144
	BL2	60	75	**120**
4 lane	BL8	**40**	50	**80**
	BL4	36	45	72
	BL2	30	38	60



FEATURES

- 1152Mb 1T-SRAM® memory array architecture
  - 3.2 ns core cycle time
- Low-latency SerDes technology
  - 4, 8 or 16 serial transceivers (TX/RX)
  - OIF CEI-11G-SR and CEI-28G-VSR compatible
  - Tuned for low-power transmission up to 20 cm
- Open GigaChip® Interface delivers bandwidth, efficiency and reliability
  - Low latency protocol
  - Reliability with scrambling, CRC and error recovery mechanisms
- Intelligent Error Management and Bit Safe® Technology
- High reliability – 1T-SRAM soft error immunity
- Advanced debugging and evaluation capabilities with MoSys IC Spotlight software



HIGH ACCESS RATE AND THROUGHPUT

The burst mode of the MSR630 delivers full duplex effective data throughput resulting in the smallest footprint and power consumption for this performance capability.

The word size is 72 bits and the MSR630 supports up to five billion read transactions per second, ideal for random read and algorithmic processing. Through the use of table replication, the access rate can be increased two or more times.

UNIFIED MEMORY IMPLEMENTATIONS

The functionality is selectable on a cycle by cycle basis, allowing the use of the device in unified memory applications and optimizing the access patterns accordingly. Multiple tables and buffers can be defined with access interspersed between applications which could use a single , double or burst access command as needed.

BOARD DESIGN ATTRIBUTES

- 676 FCBGA, 27mm x 27mm, 1.0mm ball pitch
- 0.9V/1.0V, 1.5V, (1.8V EEPROM) supplies
- IEEE 1149.1/1149.6 JTAG boundary scan
- SPI / I2C configuration port

ORDERING INFORMATION

Base Part Number	Temperature	Speed
MSR630AA	C	-25
	E	-15
		-12

GIGACHIP INTERFACE

The GigaChip Interface (GCI) is an open, freely licensable, efficient transport layer built on compatible, industry standard SerDes. GCI is optimized for small packet, chip-to-chip communications including error detection and recovery mechanisms.

GIGACHIP FRAME FORMAT

The GigaChip Interface uses a fixed-size 80-bit frame, consisting of 72-bit payload, 6 bits of CRC and 2 control bits, providing 90% transport efficiency. Each lane is scrambled with a pseudo-random bit sequence, providing sufficient transition density and DC balance for reliable, high-speed serial communications without the overhead of 8b/10b encoding.

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