Bandwidth Engine® 2 Board Layout Guidelines

Application Note AN-607

Version 0.1, February 2014
MoSys, Inc.

Introduction

This application note describes board layout requirements and recommendations for use with the Bandwidth Engine 2 (BE-2) in a 19 mm x 19 mm package. They are generally applicable for up to 15.625 Gbps transceiver rates. This document should be used in conjunction with Bandwidth Engine 2 Board Schematic Guidelines AN-608.

Requirements are items that must be met. Recommendations are guidelines that are design best practices, and the user should either adhere to these or to equivalent alternatives.

This document contains the following sections:

- “Board Layout” on page 2
- “Board Design and Verification” on page 7
- “Board Compliance” on page 9

Definitions

Figure 1 Component overview

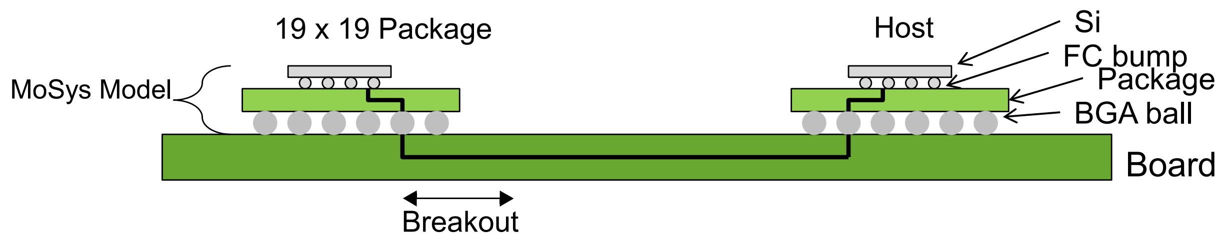


Table 1 Terminology

Term	Description
Bandwidth Engine 2 (BE-2)	The MoSys® device in 19 mm x 19 mm package.
Host	The ASIC, ASSP, or FPGA connecting to BE-2.
Flip Chip (FC or C4)	The bump connecting the chip to the package.
BGA (Ball Grid Array)	The solder ball connecting the package to the board.

Table 1 Terminology *(continued)*

Term	Description
Breakout	The routing region under the BGA and between BGA to the main board route. These routes may require special considerations such as thinner traces, plane voiding, via fields, etc. to escape out of the BGA field.
MoSys Package Model	Will include chip pad/Flip Chip bump to BGA/PCB interface.

Reference Design Kit

A reference board schematic and layout are available. These can be used as starting points.

- BE-2 Dual FMC Mezzanine Card schematic example (available as PDF file and ORCAD file)
- BE-2 Dual FMC Mezzanine Card layout example, corresponding to a TBD layer board (*.brd)

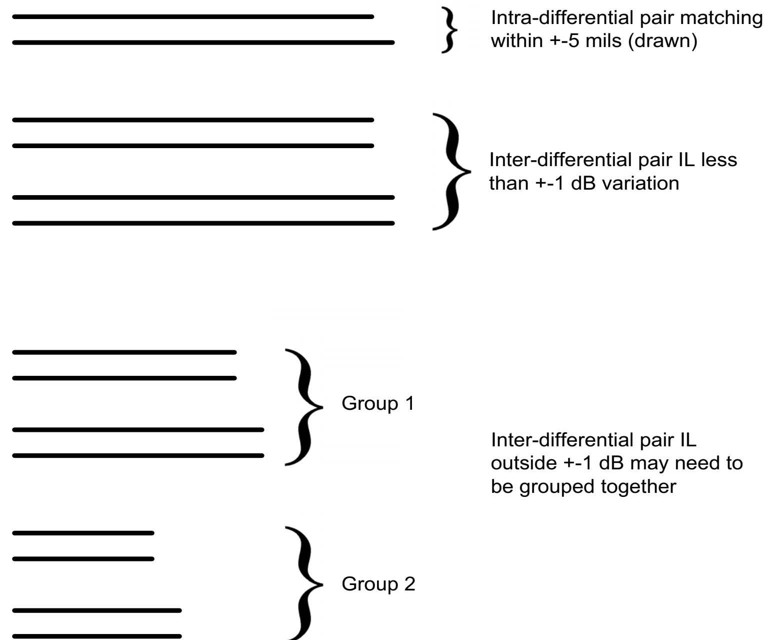
Board Layout

Signal Layout

For high speed signal layout striplines or microstrips can be used. Striplines are preferred because they have lower crosstalk, better impedance control, and lower EMI. Microstrips can be used provided overall interconnect criteria are met.

Routing signals on separate layers is acceptable, provided impedance, reflection, and crosstalk criteria are met. Keep differential pairs close to 180° out of phase.

Figure 2 Matching requirements for the board interconnect. Grouping by IL (insertion loss) may be required for optimum equalization purposes.



Loss Requirements

Table 2 Loss requirements of board

Parameter	Description
Insertion Loss	> -11 dB @ ½ x bit rate (i.e., 6.25 GHz for 12.5 Gbps) +/- 0.5 dB variation ripple from DC to ¾ x bit rate +/- 1.0 dB variation ripple from ¾ to 1½ x bit rate
Return Loss	Less than -12 dB from DC to ¾ x bit rate
Crosstalk	<-40 dB @ ½ x bit rate (to nearest differential pair)
Impedance	Zo: 100 Ω +/- 10% differential Zo: 50 Ω +/- 10% single-ended
Matching	Differential pairs drawn +/- 5 mils in length Lane variation less than +/- 1 dB per group

Reference Clock and Miscellaneous Signal Routing

Use the following recommendations for reference clock and miscellaneous signal routing:

Reference Clock

- The reference clock should be routed as a differential pair, with a differential impedance of 110 Ω +/- 10% to match the reference clock termination resistance of the Bandwidth Engine 2 device.
- Isolation of -60 dB to any other signal is recommended.

Miscellaneous Signals

- Miscellaneous signals that must be routed as 50 Ω are EVENTA#, EVENTB#, SS#_I2C_SADR0, SDO_I2C_SDA, SDI_I2C_SADR1, SCLK_I2C_SCL, . It is recommended that the EVENT pins be routed on as short a trace as possible back to the controller. The trace delay for the EVENT signals needs to be no more than 2.5 to 3.0ns to minimize the timing delay from EVENT# to the host controller recognizing EVENT#.
- Miscellaneous signals RESET#, CONFIG#, CLKDIVIDE, I2C_SPI_SEL, I2C_SADR2 are static and do not need to be routed as 50 Ω. READY# is a very slow switching signal and does not need to be routed as 50 Ω.

The reference for both of the above should be ground.

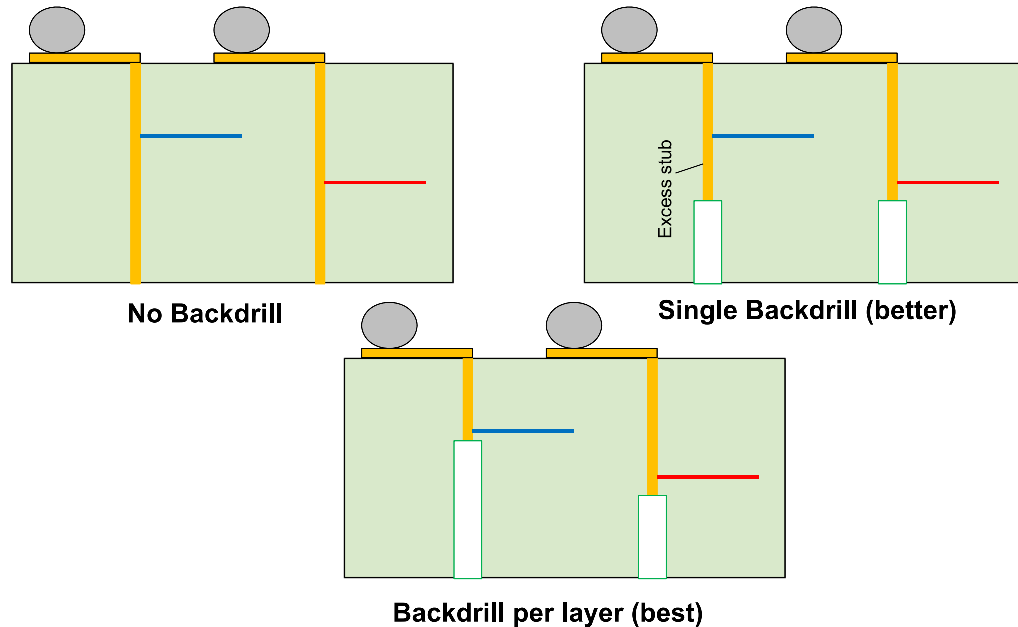
Backdrill Recommendation

The following are backdrill recommendations:

- Backdrill may be required to meet the return and insertion loss of Table 2 on page 3.
- Backdrill to within 10 mils of signal layer is recommended.
- Backdrill per signal layer may be required, keeping the stub within 10 mils. This is the best and recommended option.

See Figure 3 for backdrilling options.

Figure 3 Backdrill recommendation

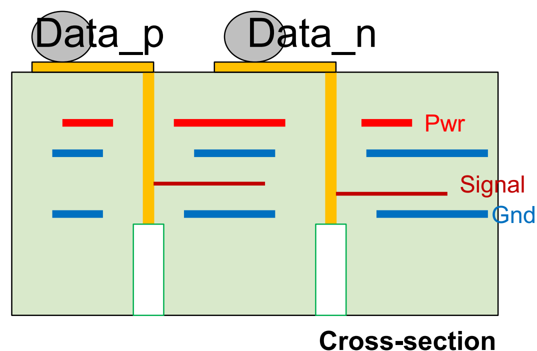


Via Recommendation

Vias need to form a 50 Ω impedance transmission line. Some guidelines:

- May require voiding of Pwr/Gnd plane directly under the BGA pad.
- Via placement (diff pair) are typically at the same pitch as BGA, 1mm.
- Via diameter: ~10-14 mil diameter
- Anti-pad sizing: ~30-35 mil diameter
- Usually a design may have more Vss planes, relative to the number of power planes. In such a case, the ground anti-pad can be larger than the power plane.
- Consult the layout in the design kit for a detailed example.

Figure 4 Via recommendation

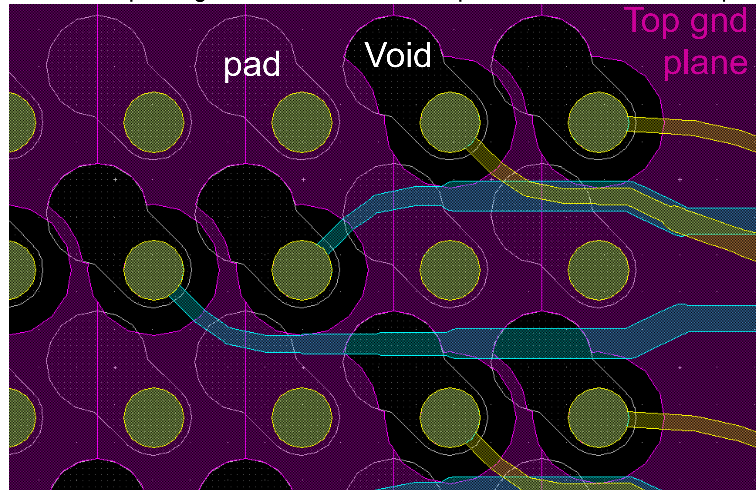


Ground Void Recommendation

BGA pads should be as small as manufacturing permits to help reduce excess capacitance. The Ground/Power directly under the pad may be voided as shown in Figure 5. This voiding reduces vertical capacitance between the BGA pad and the ground plane(s). If required, the top few planes may be voided.

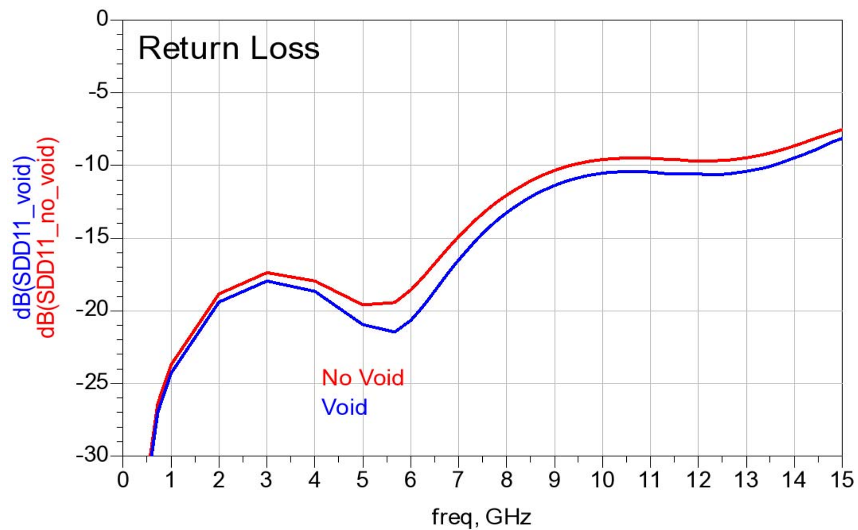
Note: Usually an anti-pad may be in the same layer as a pad. It is the gap between the pad metal and the plane in the same layer. Void is a hole in the plane, with the idea of reducing vertical capacitance.

Figure 5 Example of ground void to reduce capacitance between BGA pad and ground.



An example of ground void reducing the return loss is shown in Figure 6.

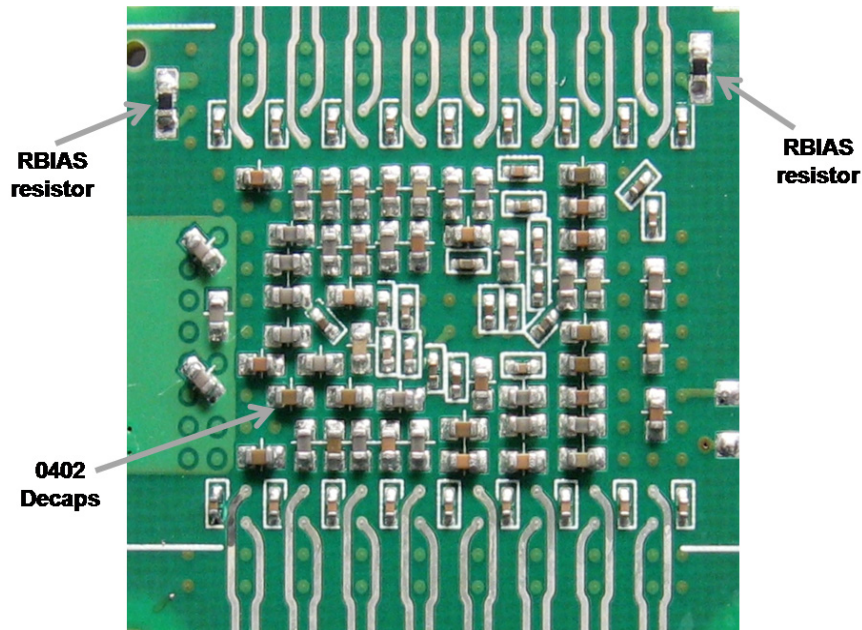
Figure 6 Example of ground void reducing return loss.



Bias Resistor Placement Requirement

It is recommended that the bias resistors be placed adjacent to or directly underneath the BE-2 device as show in Figure 7. The capacitance (board trace, and pad) must be < 2pF.

Figure 7 Bias resistor and decap placement



Power Routing Recommendations

- Place VDD and VSS vias adjacent as a pair. Add as many VDD-VSS core via pairs as required.
- Use planes for all power supplies.
- Recommend using the top most (or towards the top) plane for VDDA_SDS supply which will lower loop inductance.
- Populate decap under the component for most VDD and VSS balls adjacent as a pair.

Decap Placement Recommendation

Figure 7 shows recommendations for decap placement.

Board Layout Recommendations

Following are board recommendations:

- GCI specification permits a range of interconnect skew that are leveled within the component, but more skew causes more insertion loss mismatch. Also, a design that uses low skew might be able to use the same equalization settings on all lanes. The

overall equalization programming strategy is that available link margins should be simulated, and the allowable mismatch in insertion loss estimated. For example, when the link margins are smaller, the insertion loss of the link should be matched tightly, or each lane should be programmed. However, if there is sufficient link margin, more interconnect loss skew may be acceptable, or coarser equalizer programming is acceptable.

- Make interconnect length matching per Table 2 on page 3. Each group may need to be optimized for equalization if the channel is near its limits.
- The board must minimize discontinuities, in the form of excess capacitance or inductance, that cause large deviations from Zo.
- Back drilling of thicker boards is recommended to meet return loss.
- Use ground voids to reduce capacitance between BGA and ground and resulting return loss, as shown in example in Figure 6.

Board Design and Verification

Measurement Setup Model

The measurement setup defines measurement points and insertion and return loss, whether they are from

- Extracted models of boards and packages
- Compilation of cascaded models (extracted or measured)
- Measurement setup

The interconnect setup should include package and board along with associated parasitics. Normal applications will use soldered parts.

Package models from vendors will be required to build this channel model. If no vendor package is available, then a reasonable package should be substituted in the interim. However, for final tapeout, the actual package models are required.

All SerDes signals must be referenced to a common ground. This is important as all the return paths are completed using Vss in the package.

The highest operating data rate of the links is 15.625 Gbps but customers may operate at a lower bit rate. The Nyquist frequency corresponds to 50% of the operating bit rate. For return loss, a corner frequency of ¾ x baud rate is also defined.

Figure 8 Setup of board for insertion and return loss characterization.

The Bandwidth Engine 2 19x19 mm^2 package model is supplied in the IBIS-AMI model supplied by MoSys.

In addition to S-parameter measurements, it is highly desirable to perform a TDR analysis of impedance versus time (or length). This will identify any major discontinuities.

Board Power Supply Design and Power Delivery

Power Integrity Recommendations

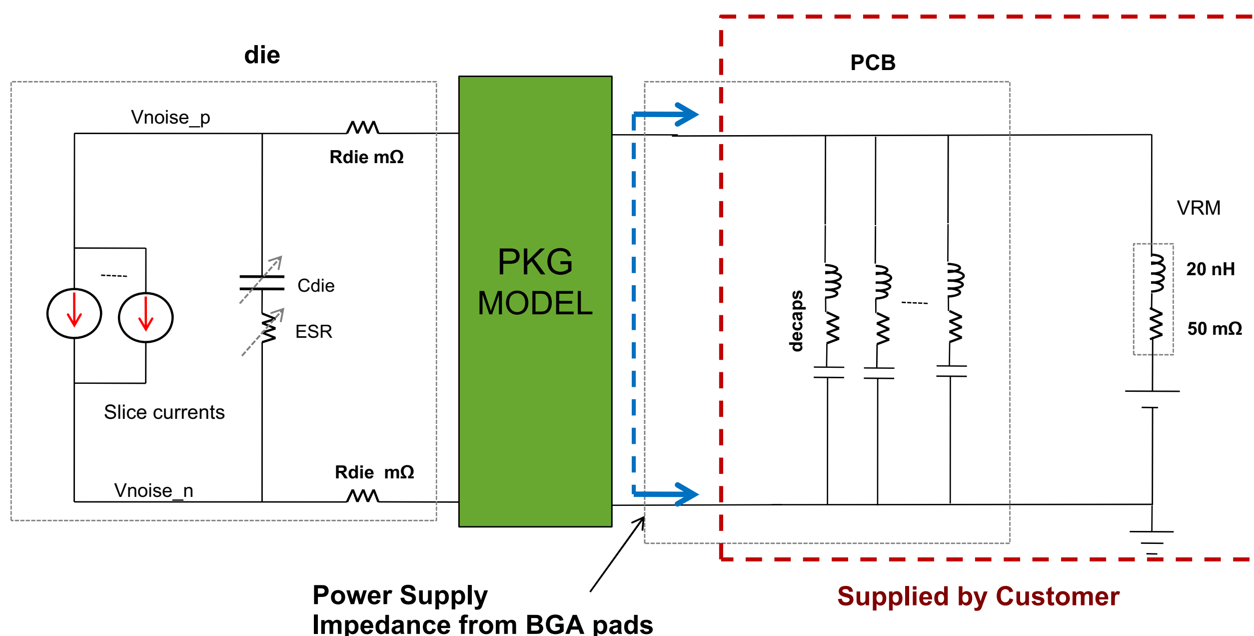
The VDDA_SDS (SerDes analog power supply) power supply has a tight AC ripple tolerance, so care must be taken to reduce loop inductance in the board.

Loop inductance can be reduced by following the routing recommendations in , “Power Routing Recommendations,” on page 6

Typical Test Bench for the Power Model

Figure 9 shows a typical test bench for the power model.

Figure 9 Typical test bench for the power model



VRM parasitic provided are representative values. For actual values consult your VRM vendor.

Power Sharing and Delivery

See Bandwidth Engine 2 Board Schematic Guidelines AN-608 for detailed power supply and power sharing recommendations. It describes two methodologies for estimating the decoupling capacitor requirements on a board. The second method discussed uses the target impedance values shown in Table 3. The power supply requirements are different for -10, -12, -14, and -15 speed devices as shown in Table 3.

Table 3 Bandwidth Engine 2 power delivery requirements

S. No.	Power Supply Domain	Nominal DC Voltage (V)	DC Tolerance	Max AC Ripple at BGA balls (mV p-p)	Recommended Ztarget[1] at BGA balls (mΩ)
1	$VDDA_SDS_{-10}$	0.90	±5%	15	100

Table 3 Bandwidth Engine 2 power delivery requirements *(continued)*

S. No.	Power Supply Domain	Nominal DC Voltage (V)	DC Tolerance	Max AC Ripple at BGA balls (mV p-p)	Recommended Ztarget[1] at BGA balls (mΩ)
	$VDDA_SDS_{-12}$	0.95	±5%	15	100
	$VDDA_SDS_{-14}$	1.00	±3%	15	100
	$VDDA_SDS_{-15}$	1.01	±2%	15	100
3	VDDHV_SDS	1.5	±5%	15	400
4	VDD_{-10}	0.90	±5%	20	50
	VDD_{-12}	0.95	±5%	20	50
	VDD_{-14}	1.00	±3%	20	50
	VDD_{-15}	1.01	±2%	20	50
6	VDDHV	1.5	±5%	25	400

1. Fmax = 100 MHz

Board Compliance

Customer Board Compliance

Following are customer board compliance recommendations. Customers are encouraged to have all or subset of these board and packages available. Using these boards and packages can quickly establish if the board and packages meet the design guidelines.

Board Compliance Check

- Measure board S-parameters from 10 MHz to 1½ x bit rate (i.e., 18.75 GHz for 12.5 Gbps).
- Insert measure channels into a compliance simulation (see “Measurement Setup Model” on page 7).
- Blocks not available for measurements should be included in a simulation model, and the insertion, return loss and cross talk extrapolated.

Package Compliance Check

- Have blank packages with BGA balls available, where feasible.
- Measure package S-parameters from 10 MHz to 1½ x bit rate (i.e., 18.75 GHz for 12.5 Gbps).

Assembled Board Compliance Check

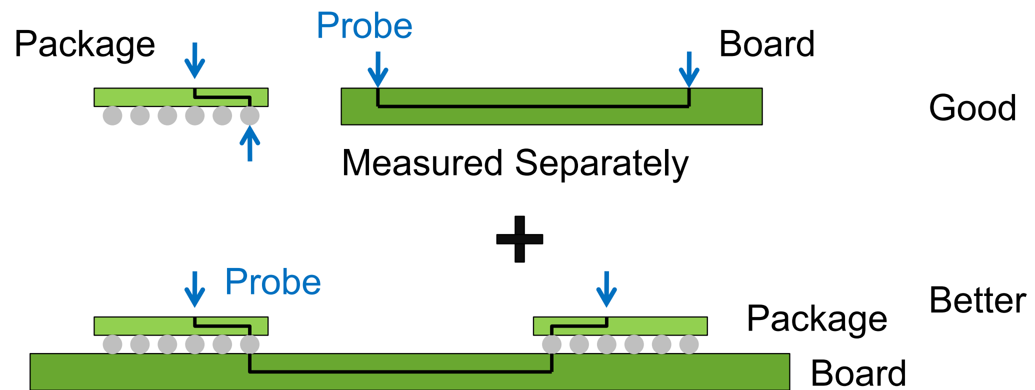
- Mount package(s) on board, and measure the S-parameters of representative channels.
- If a socket is required, it should be measured in the channel.

Compliance Board Setup

Compliance board setup recommendations include:

- Four port differential measurements are recommended.
- Insertion and Return loss, and cross talk should be measured.
- Individual component s-parameter measurements are required. Some may be obtained from the vendors, or other emulation done.
- An assembled board setup is recommended in addition to individual measurements, provided the components are available from vendors. This measures the discontinuities.

Figure 10 Compliance board setup



MoSys

Version History

Date	Version	Changes
February 2014	0.1	Initial release.

2/27/14

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