MoSys Newsletter
Accelerating Data Intelligence
www.mosys.com
Vol 1 No. 2, June 2020

A Message from MoSys

Welcome to the second edition of the MoSys newsletter. The world as we know it continues to shelter in place as we all do our part to ensure that our customers continue to have access to the industry's most innovative acceleration solutions. In this issue:

- Focus Technology: FPGA internal memory or external SRAM, or better yet…both.
- Other Technology: High Speed Board Design Guidelines… Signal Integrity of Stripline or Microstrip.
- We have collaborated with PBS's The Information Matrix to bring you a short video discussing the latest technology advancements from MoSys. The show is hosted by Lawrence Fishbourne and we cover the exciting new progress in acceleration tech poised to take your applications to the next level. We have a sneak preview here that you can view: LINK

So welcome *to the second edition of our newsletter where we will continue to keep you up to date on all things acceleration, memory, and of course, MoSys.*

Featured Content:

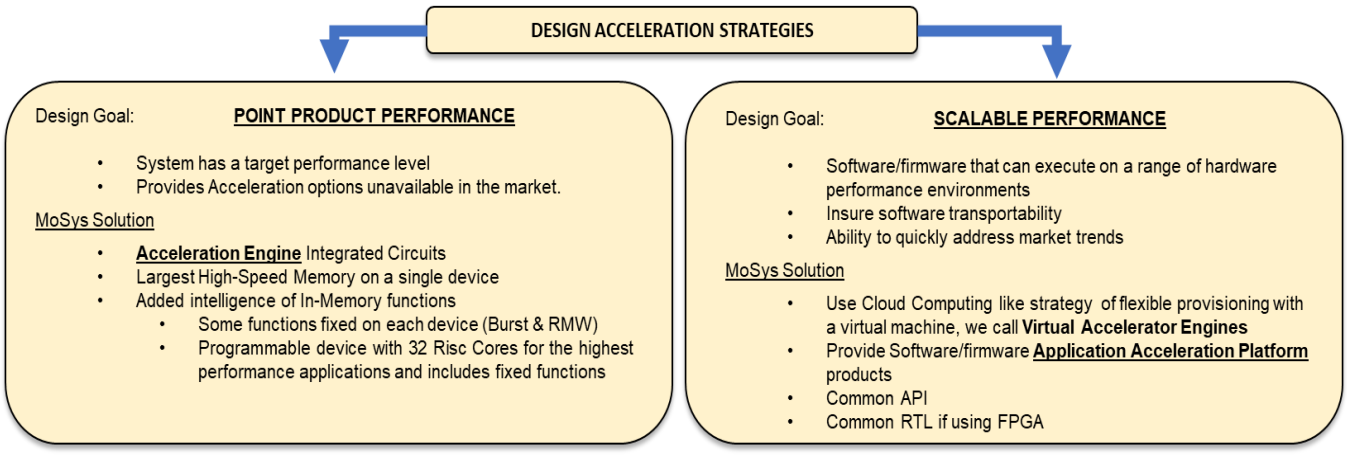
- Packet Classification Apps Just Got a Whole Lot Easier to Manage
- Put Your Development Efforts on Auto Pilot with MoSys RTL
- MoSys LineSpeed™ Flex PHY Solutions – Successful Design and Bring-Up of a Serial Link
- Digi-Key and Mosys: A Powerful Combination

News Alerts!

MoSys Announces Global Distribution Agreement With Digi-Key Electronics
Mar 3, 2020
MoSys Releases New LineSpeed(TM) 100G PHY Design Support Package
Jan 28, 2020
MoSys Announces New Software Targeting Packet Classification Applications
Jan 14, 2020

New Blogs:

- There is a New Type of Memory in Town Part I
- There is a New Type of Memory in Town Part II
- Solving Bottlenecks, Let's Do the Math
- Dense 10GbE Breakout with MoSys LineSpeed™ Flex PHY
- Cyber Security in Turbulent Times Part I
- Cyber Security in Turbulent Times Part II
- Save 2-8 System Operations with In-Memory Functions (BURST) Part I
- Save 2-8 System Operations with In-Memory Functions (RMW) Part 2
- Two Roads Diverge: How To Accelerate Your Future Part I: Hardware
- Two Roads Diverge: How to Accelerate Your Future Part 2: Software



Solution Note 1004

MoSys Design Support Center

How Bandwidth Engines Complement FPGA BRAM, uRAM, and M20K

It is easily understood that it is advantageous to use resources (in this case, memory) that is close and localized to a source of a data request. Even with the on die real estate becoming increasingly valuable, chip companies are dedicating significant resources to memory.

- Xilinx
  - BRAM (a distribution of smaller blocks of ram across the die)
  - uRAM, larger blocks of RAM (in columns of the die)
- Intel (Altera) use a hybrid of the Xilinx model
  - M20K blocks, similar to BRAM (distributed across the die)

Both approaches have some routing and timing restrictions when the desire is a large unified block of memory, however they do have SRAM speed benefits.

However, there are times when a large off FPGA SRAM, such as 567Mb or larger can be beneficial.

- External memory can simplify timing and routing
- More high-speed memory allows more data to be close to the FPGA for processing
- Allows more real time data handling over DRAM/RLDram approaches

As long as the memory does not interfere with other resource requirements of the FPGA and the size of the memory needed does not result in difficult routing and timing, the benefits are tremendous.
The key is to look at how, together, they ***complement*** each other to improve performance and simplify the design. Having a single chip 567Mb or 1Gb memory attached to an FPGA allows more choices regarding FPGA system memory architecture and performance tradeoffs. Not an easy decision!

Read Full Solution Note: LINK
OR find out more, Contact: AppSupport

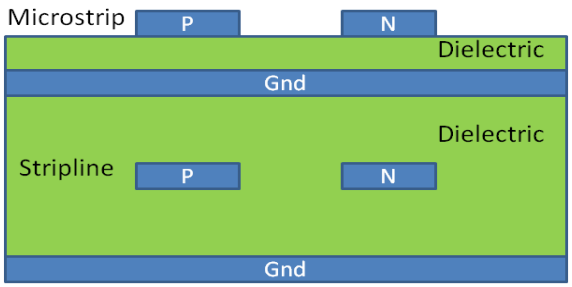
More Technology – "High Speed Board Design Guidelines'

Up Next: Signal Integrity

To connect the differential pair to its counterpart in another device, stripline or microstrip could be used. The cross-section below illustrates the two.

- Advantage of microstrip
  - Can eliminate vias between the two devices if the routing is done on the top surface.
  - Using microstrip eliminates the need for backdrill if routing is constrained to top and bottom of the PCB.
- Disadvantes of microstrip
  - Due to the coupling mainly down to the ground underneath, the majority of the conduction in the trace is constrained to the bottom layer due to skin effect
- Advantage of stripline
  - Conduction can spread to both the top and the bottom of the traces, enabling lower conductive loss for a given pitch.
- Disadvantages of stripline
  - Special plating of outer copper layers and solder mask may cause high frequency losses.

Other components on the board that may not be known or characterized at the time of the board design may affect the trace impedance too (e.g. sockets, stiffeners, mats put on surface during testing etc). Read more: LINK To "High Speed Board Design Guidelines"



ADDITIONAL RESOURCES

- ❖ Webinar: VAE
- ❖ White Paper: Virtualized Acceleration
- ❖ White Paper: Chiplet Interconnect – Parallel or Serial?
- ❖ Solution Note: Buffering up to 800 Gbps throughput w/ Bandwidth

Email us and we will arrange to have one of our technical specialists speak with you. You can also sign up for updates. Finally, please follow us on social media so we can keep in touch.