MoSys Newsletter
Accelerating Data Intelligence
www.mosys.com
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A Message from MoSys CEO Dan Lewis

Times, as we all know, are unprecedented. Catch phrases like sheltering in place, social distancing were all unheard of just a few months ago.

So we begin two new relationships:
- MoSys Newsletter to keep you up to date.
- MoSys agreement with Digi-Key to provide you technical support and product availability.

We are excited to be associated with such a successful and powerful global distributor that can provide MoSys a way to reach markets and customers unattainable before.

And, as one of Dig-Key's premier customers, you now have access to our Accelerator products that can improve your product performance significantly.

So welcome *to our brand-new newsletter where we will be keeping you up to date on all things acceleration, memory, and of course, MoSys.*

New Blogs:

- 5 Reasons You Should Consider Adding Acceleration Tech to Your Apps Now
- The Benefits of Serial Memory
- Supporting 4 x 100GE TCAM vs Algorithm-Based Solution Use GME
- How Accelerating Big Data and Virtual Acceleration Technology Can Save the Day in a Pandemic
- Speeding Up Your FPGA/ASIC Memory Interface (GCI)

News Alerts!

MoSys Announces Global Distribution Agreement With Digi-Key Electronics
Mar 3, 2020

MoSys Releases New LineSpeed(TM) 100G PHY Design Support Package
Jan 28, 2020

MoSys Announces New Software Targeting Packet Classification Applications
Jan 14, 2020

Featured Content:

- Packet Classification Apps Just Got a Whole Lot Easier to Manage:
- Put Your Development Efforts on Auto Pilot with MoSys RTL
- MoSys LineSpeed™ Flex PHY Solutions – Successful Design and Bring-Up of a Serial Link
- Digi-Key and Mosys: A Powerful Combination
- MoSys LineSpeed™ Flex PHY Solutions – Successful Design and Bring-Up of a Serial Link

DESIGN ACCELERATION STRATEGIES

Design Goal: **POINT PRODUCT PERFORMANCE**

- System has a target performance level
- Provides Acceleration options unavailable in the market.

MoSys Solution

- **Acceleration Engine** Integrated Circuits
- Largest High-Speed Memory on a single device
- Added intelligence of In-Memory functions
  - Some functions fixed on each device (Burst & RMW)
  - Programmable device with 32 Risc Cores for the highest performance applications and includes fixed functions

Design Goal: **SCALABLE PERFORMANCE**

- Software/firmware that can execute on a range of hardware performance environments
- Insure software transportability
- Ability to quickly address market trends

MoSys Solution

- Use Cloud Computing like strategy of flexible provisioning with a virtual machine, we call **Virtual Accelerator Engines**
- Provide Software/firmware **Application Acceleration Platform** products
- Common API
- Common RTL if using FPGA

MoSys Design Support Center

Featured Technology:

QDR Replacement: Faster, bigger, simpler!

MoSys Accelerator Engine family was designed as a larger, higher bandwidth memory than anything on the market. It replaces QDR, Sync SRAM and RLDRAM.

Features:

- Inter-operability with Xilinx and Intel FPGAs
- Utilizes a MoSys GCI Interface.
  - Supports 4, 8 or 16 lanes of SerDes
  - SerDes can operate up to 25Gb/s
  - BE-2 has 576 Mb of memory on a single device
  - BE-3 has 1 Gb of memory on a single device

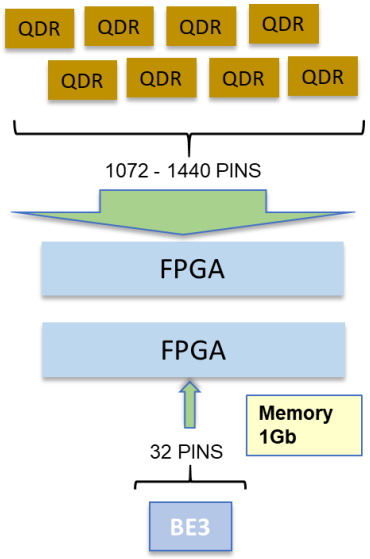
Device Equivalents	Storage	Costs $	FPGA Signal Pins	Bandwidth Gb/s
BE2	576 Mb	2 QDRs	32	320
4 - QDR - 144 Mb	576 Mb	4 QRSs	~700	190
BE3	1 Gb	3 - QDRs	32	640
8 - QDRs - 144 Mb	1 Gb	8 - QDRs	~1440	190

How can we be

- Faster
- Cheaper
- And still have higher bandwidth?

To find out

Contact AppSupport



More Technology:

High Speed Board Design Guidelines

No one likes designing high speed boards. Signal integrity issues are everywhere. Trace length, routing pattern, signal ringing, impedance mismatch and it goes on.

MoSys has years of experience designing high speed products and helping customers design their boards. This application note covers all you need to know, and then some…

Some of the Features:

- Material selection and stackup
- Impedance characteristics and control
- Cross-talk
- Skew and risky routing
- Delay matching with a wiggle pattern
- **Request Guidelines**

Be sure to ask about MoSys Bandwidth Engine's Auto-Adaptation to eliminate board components.

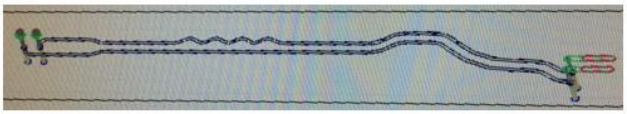


Figure 17: Differential trace between BGA (left) and QSFP28 (right)

Benefits of Serial Memory – Mosys GCI

Can a MoSys memory with 32 serial signal pins have higher bandwidth than QDR 1440 parallel signal pins?

Yes!

Memory Serial Features:

- A MoSys protocol with 90% efficiency
- Mosys memories SerDes speed from 10.5-25 Gb/s
- Easy to understand FPGA RTL Requirements
- *Interfaces with MoSys supplied RTL memory code for Intel and Xilinx so you do not have to write a serial RTL interface…unless you want to!*
- **Mosys RTL Memory Controller** **Download**

Featured Posts:

Digi-key…We've Teamed Up!

MoSys signs Digi-Key Electronics, a world's leading electronic component distributor. Read more…

Security in a Pandemic world!

Big Data and Data Intelligence are key in a Pandemic situation. Read more…

Additional Resources:

- Webinar: VAE
- White Paper: Virtualized Acceleration
- White Paper: Chiplet Interconnect – Parallel or Serial?
- Solution Note: Buffering up to 800 Gbps throughput w/ Bandwidth Engine Memory

Email us and we will arrange to have one of our technical specialists speak with you. You can also sign up for updates. Finally, please follow us on social media so we can keep in touch.