## SOLUTION OVERVIEW

The MoSys Cheetah Development Kit provides an integrated Xilinx FPGA and tightly coupled low latency BE-3 or BLAZAR PHE (Programable HyperSpeed Engine) reference environment to enable quick implementation of any algorithms that are offloaded from the FPGA. The solution can be executed in a PHE device using the PHE's 32 RISC cores for accelerated performance.

❖ The Cheetah is a full height, full length PCIe form factor that can plug into servers. Has 2 x 100G QSFP28 interfaces.
❖ Cheetah offers the ability to offload functions and algorithms into the PHE. This frees up resources in the FPGA that are better suited for higher priority functions, enabling designers to add system functionality.
❖ The MoSys device can also serve as a replacement for multiple QDR devices. It is a 1Gb high-speed random-access memory with up to 5G accesses/sec in one device.
❖ Reference design is available for review and/or use now.
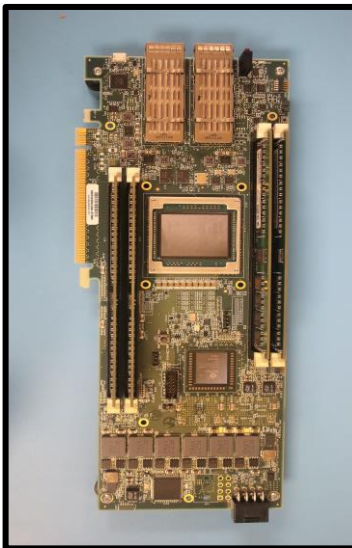
This solution provides designers the flexibility to tailor a solution and address a 10x to 100x performance improvement over traditional FPGA implementations.
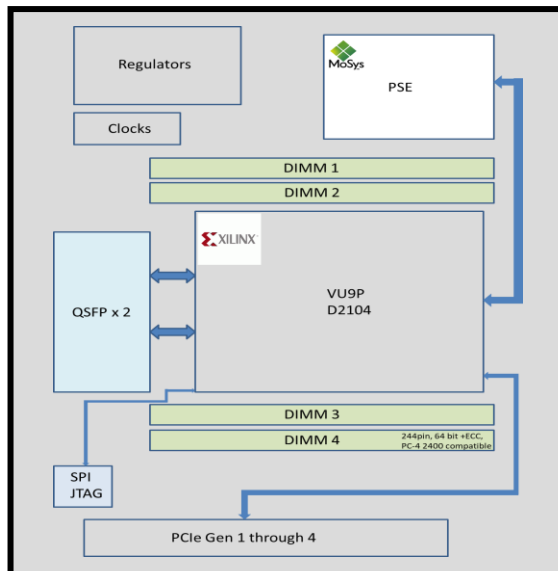
APPLICATIONS AND USE CASES:

❖ Network Monitoring
❖ Intrusion Detection
❖ IPv6/LPM
❖ ACL
❖ Load Balancing
❖ Data Analytics
❖ Reg Ex
❖ High-Speech Data Collection
❖ Genomic Algorithms
❖ Bitcoin
❖ Video Processing
❖ DPI/OVS/NFV
❖ Traffic Switching
❖ High Speed Testing
❖ High Speed Parallel Processing
❖ Graph Memory

KEY FEATURES of the DEV KIT / REFERENCE DESIGN

❖ Utilizes a Xilinx XCVU9P device
❖ *Includes a MoSys BE-3 or PHE (Programmable HyperSpeed Engine)*
❖ Supports all Xilinx 1525 applications
❖ Dual Slot PCIe compliant (Full Height and Length)
❖ MoSys PHE directly attached to Virtex UltraScale+ SerDes
❖ 16 lanes of 25G SerDes to PHE allowing full bandwidth up to 400Gbps full duplex.
❖ 1Gb of high-speed memory which can be utilized as an extension to the FPGA resources
❖ Uses only 40K LUTs to interface with PHE
❖ 64 GB of DDR4
❖ PCIe Edge Connector
❖ Micro USB Port and two QSFP28 ports

MOSYS SOFTWARE DEVELOPMENT SUPPORT

❖ IDE (Integrated Development Environment) which allows for Lynx based development and debug.
❖ Spotlight (Windows-based) environment that allows for setup and debug of the MoSys device through SPI.
❖ Supports a full development and debug environment.

# MoSys Programable HyperSpeed Accelerator Engine (PHE) Architecture

The BLAZAR family of Accelerator Engines (AE) provide a balance of High-Speed Random-Access Memory and Embedded In-Memory Functions. The combination of the two allow the hardware and software system designer to accelerate the performance of an FPGA-based application.

The AE's memory has embedded functions that execute considerably faster "In Memory" vs. traditional memory devices. All the members of the MoSys AE family provide Fixed BURST Functions and Fixed RMW functions.

This reference design also supports the PHE which has both the BURST and RMW functions while adding the power of Embedded User Programmable Functions with the 32 RISC Cores. Users can activate any number of cores which can run in parallel.

AEs combine all of this capability with the MoSys high-speed serial protocol I/O interface operating up to 25Gbps, enabling applications to achieve HyperSpeed performance.
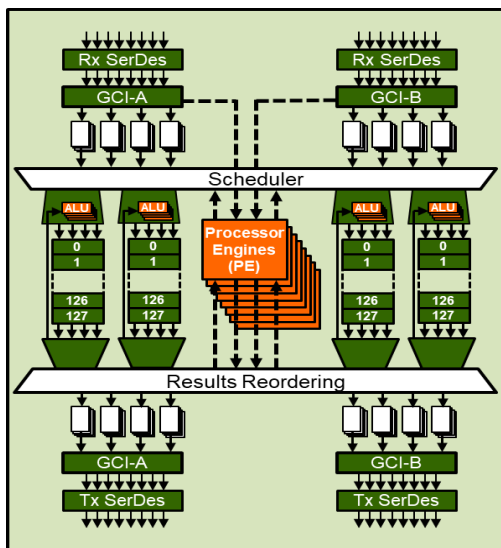
BURST Functions

The BURST Functions are focused on data movement. They accelerate getting data in and out of the memory faster and more efficiently by reducing overhead cycles.

The BURST functions are designed to nearly double the amount of data that can be moved in the same unit of time when performing individual accesses.

RMW Functions

The RMW functions are focused on data computing where there is need for memory location modification such as counting, statistics, and metering updates.

Normal memory location modification requires one command to READ a memory location, a second operation to MODIFY the value, and a third command to WRITE the new value back to the memory location. MoSys RMW commands perform this same operation in a single function call.

Programmable User Functions

The 32 RISC cores (PE - Processing Elements) are tightly coupled to the internal (both local and global) memory resources.

- ❖ Local PE Memory:
    - ▪ 32kx72b,
    - ▪ Latency of 6ns to 12ns,
- ❖ Global Main Memory:
    - ▪ 1Gb of 1T-SRAM
    - ▪ Latency of ~25ns.
    - ▪ tRC = 2.6ns

Each RISC engine has:
- ❖ 1K words of instruction memory, which can be unique or a duplicate of other processors in the processor pool for parallel execution
- ❖ Multiple scheduling domains to manage possible execution conflicts
- ❖ Each PE supports 8 thread capability (Total of 256)

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