MSH321 – LineSpeed™ 100G Multi-Link Gearbox

PRODUCT BRIEF

MSH321 DEVICE OVERVIEW

The MoSys® LineSpeed 100G Multi-Link Gearbox (MLG) is a single chip CMOS device that enables high-density, independent 10Gb Ethernet interfaces to be multiplexed into a single 100G (4x25G) interface.

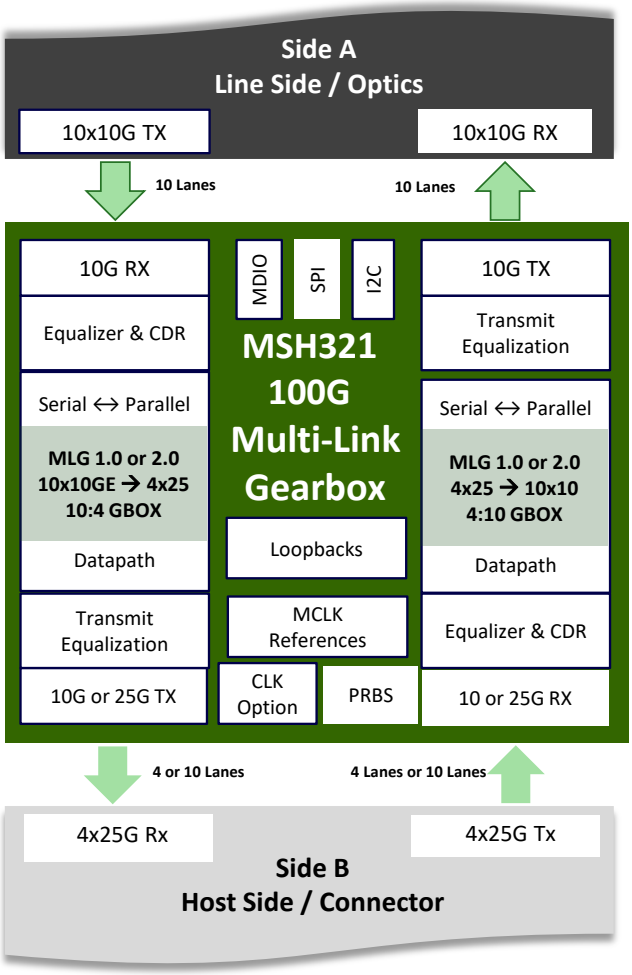
The device supports the OIF MLG-1.0 standard that aggregates 10GbE links, up to 100G total bandwidth, and converts that to a single 100G (4x25G) MLG link. As physical interfaces on switching and packet processing ICs move to 25G PHY interfaces for performance and board density, the MLG function allows large scale systems built with these devices to support higher port counts of 10GbE interfaces.

MSH321 DESCRIPTION

The MSH321 100G MLG Gearbox device performs all alignment marker insertion and awareness, idle insertion and deletion for clock rate matching, and data alignment required by the OIF MLG standard. The MSH321 also supports IEEE802.3ba standard gearbox function (CAUI-10 to CAUI-4) and optional 4x25G Retimer function. The electrical interfaces support IEEE and OIF-CEI-3.0 10/11G and 25/28G specifications.

Configuration of the device is supported through an I2C, MDIO or SPI interface and can be configured through a uC or external EEPROM.

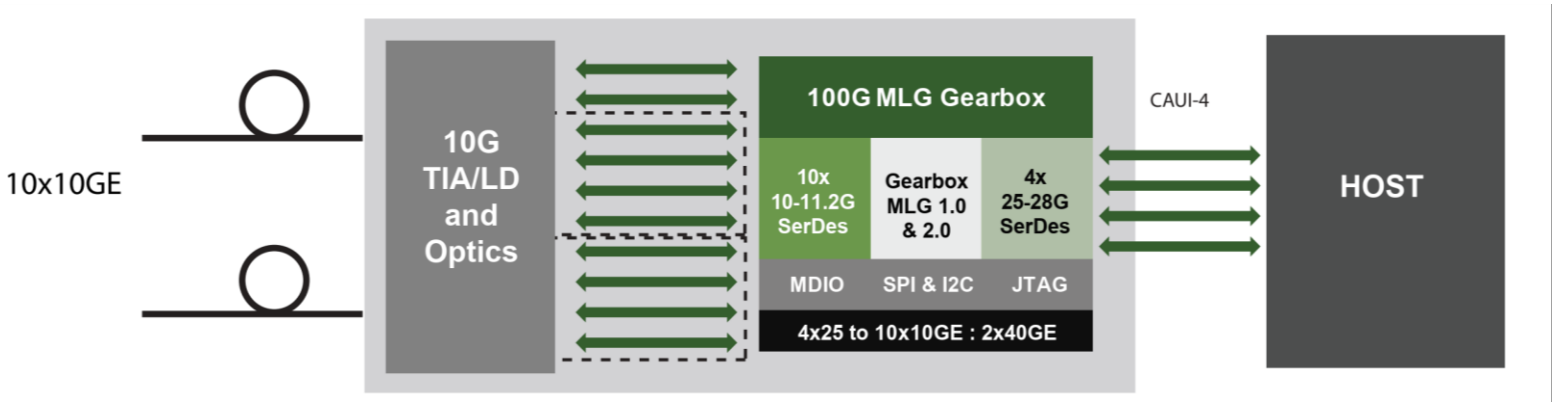
The device supports extensive test and monitor functions including PRBS Generators and checkers, error and eye quality monitors, alarms, and MLG link monitor registers.



FEATURES

- Supports OIF MLG 1.0 Standard:
  - 10 Independent 10GbE links into 100G (4x25G)
- Optional IEEE 802.3ba Gearbox for Ethernet and OTN
- IEEE and OIF 10, 25, and 100G electrical standards
- Self adapting equalizer - eye opening capability
- Transmitter and TX pre-emphasis
- Per lane PRBS generator and bit error rate checker
- Reverse polarity control on all inputs and outputs
- Monitor and reference clock support
- Base register configuration and FW provided for ease of use
- Small 12x12mm FCCSP package supports module applications

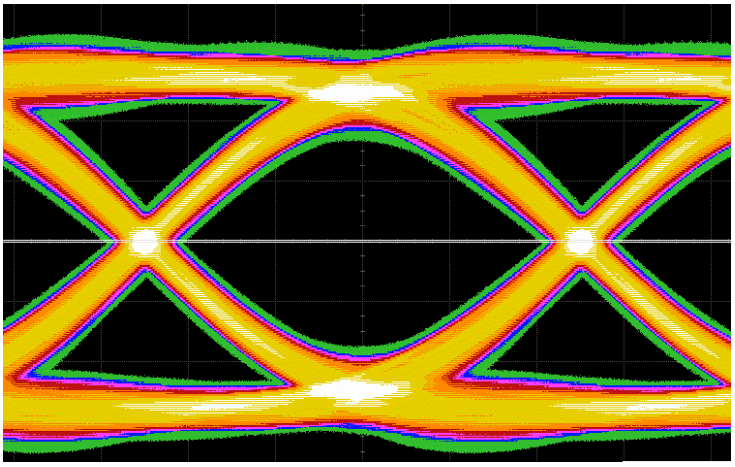
MSH321 APPLICATION EXAMPLE



MSH321 DEVICE SIGNAL INTEGRITY

To ensure signal integrity for 10G and 25G interfaces, the MSH321 has the following circuits:

- Opening the eye: A combined analog and digital RX equalizer
- Retiming: A data slicer plus a clock and data recovery circuit
- Bit stream alignment: Deserializer, frame sync and deskew functions
- Clock synchronization: An elastic buffer for data alignment
- Pre-distortion compensation: A serializer and transmit equalization circuit



PACKAGING

- 12mm x 12mm 529 FCCSP (0.5mm)

MoSys
3301 Olcott Street
Santa Clara, CA 95054
Tel: 408 418-7500
Fax: 408 418-7501

For more information
www.mosys.com