



LineSpeed™ Flex MSH320

100G Gearbox with RS-FEC

PRODUCT BRIEF

MSH320 DEVICE OVERVIEW

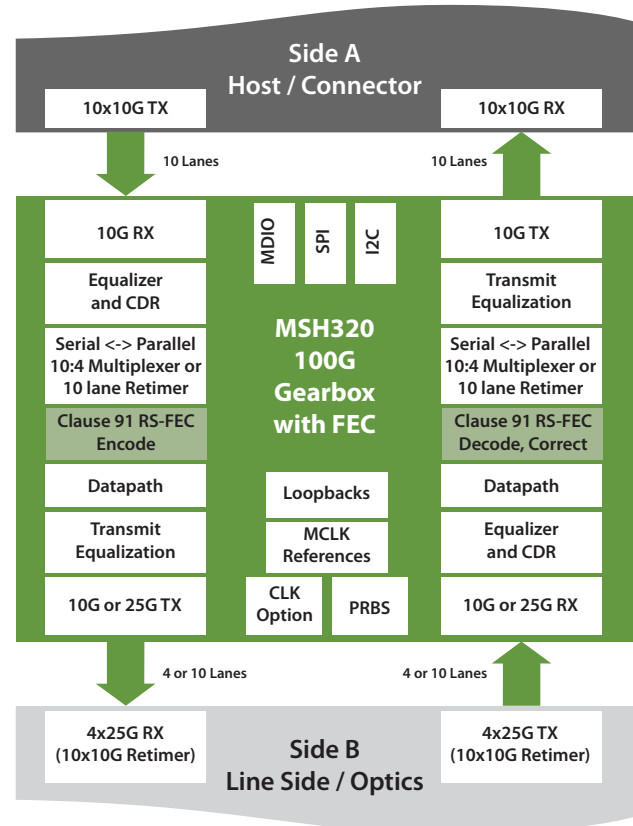
The MoSys® LineSpeed Flex 100G Gearbox with RS-FEC translates 10G interfaces to 25G interfaces, multiplexing 100G traffic at 10x10G to 4x25G. The device can support an optional IEEE 802.3bj Clause 91 RS-FEC, retimer mode for 10x10G and higher OTN rates.

MSH320 DEVICE DESCRIPTION

The MSH320 supports the IEEE802.3ba gearbox function. The electrical interfaces support IEEE and OIF-CEI-3.0 10G and 25/28G specifications. With the 100G 802.3bj RS-FEC encode, decode and correction functions enabled, the device will encode data into the 4x25G Tx interface and decode and correct data (if needed) from the 4x25G Rx interface. The IEEE 802.3bj RS-FEC enables additional signal integrity and/or distance capability over optical or copper interconnects and has been specified in multiple standards and MSAs including 100GBASE-SR4, CWDM4 and PSM4. The device can also be configured as an optional retimer for this option the device can support up to 10 independent 10G interfaces for Ethernet or OTN.

The device requires two supplies of 1.5 and 0.9V, typically. Configuration of the device is supported through an I2C, MDIO or SPI interface. The device supports extensive test and monitor functions including PRBS Generators and checkers, error and eye quality monitors, alarms, and RS-FEC monitor registers.

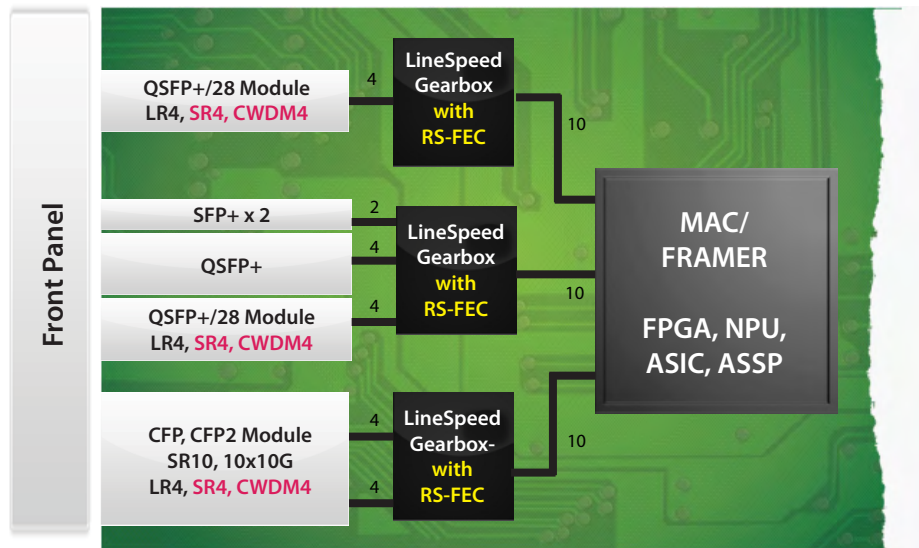
The MSH320 is well-suited for use in networking and communication applications that must support conversion of 10x10G to 4x25G and need RS-FEC for standards such as SR-4, CWDM4 and PSM4.



FEATURES

- IEEE 802.3ba Gearbox for Ethernet & OTN
- IEEE and OIF 10, 40 and 100G electrical standards
- Supports 802.3bj, Clause 91 RS-FEC Option
 - Specified in CR4, KR4, SR4, CWDM4, PSM4
- 10x10G independent retimer option
- Self adapting equalizer - eye opening capability
- Integrated Rx 100 ohm termination resistors and AC coupling
- Flexible power and configuration options
- Transmitter and TX pre-emphasis
- Per lane PRBS generator and bit error rate checker
- Reverse polarity control on all inputs and outputs
- Monitor, Alarm and reference clock support
- Internal registers can be accessed by I2C, MDIO or SPI ports
- Base register configuration and FW provided for ease of use
- Software and register compatible with LineSpeed Flex Devices

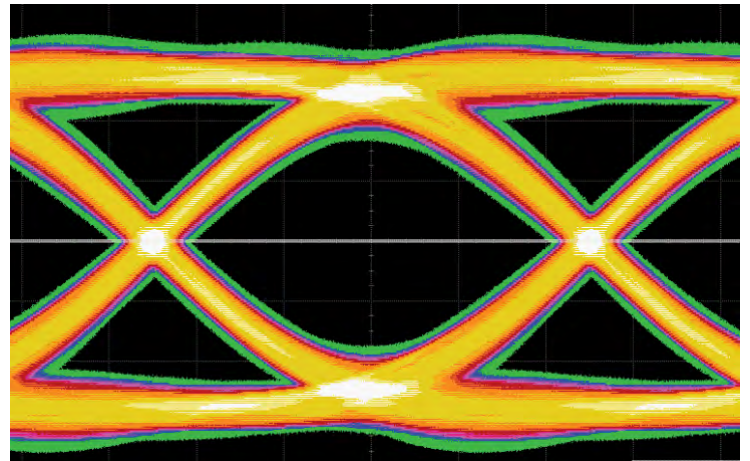
MSH320 APPLICATION EXAMPLES



MSH320 DEVICE SIGNAL INTEGRITY

To ensure signal integrity for 10G and 25G interfaces, the MSH320 has the following circuits:

- Opening the eye: A combined analog and digital RX Equalizer
- Retiming: A data slicer plus a clock and data recovery circuit
- Bit stream alignment: Deserializer, frame sync and deskew functions
- Clock synchronization: An elastic buffer for data alignment
- Pre-distortion compensation: A serializer and transmit equalization circuit
- Optional 802.3bj Clause 91 RS-FEC for 4x25NRZ for improved signal integrity
- Diagnostic capabilities to monitor and count correctable and uncorrectable FEC errors



PACKAGING

- 17mm x 17mm 256 FCBGA (1.0mm)
- Pin compatible with LineSpeed Flex 17mm devices



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