



# LineSpeed™ Flex MSH225

10 Lane Full Duplex 25G Retimer with RS-FEC

## PRODUCT BRIEF

### MSH225 DEVICE OVERVIEW

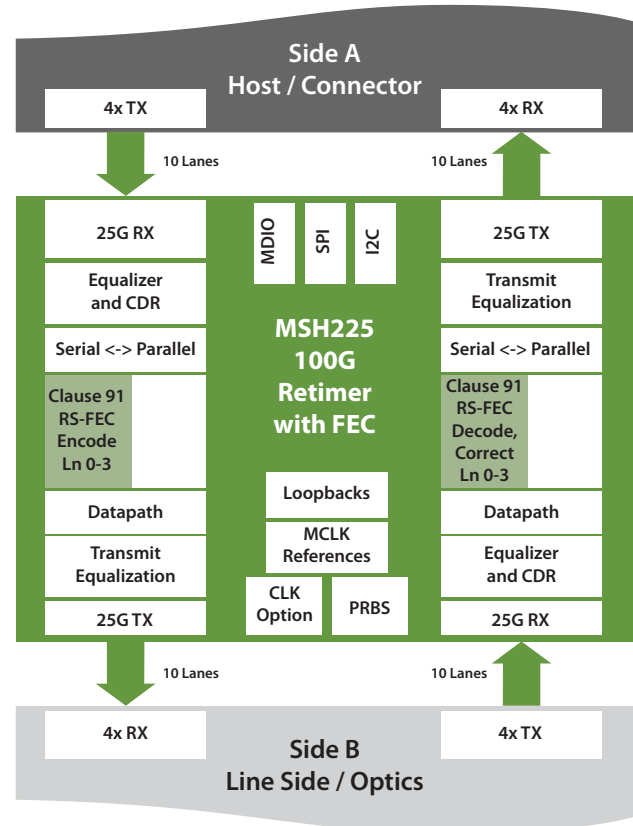
The MoSys® LineSpeed Flex 10 Lane Full-Duplex 25G Retimer with integrated RS-FEC (MSH225) is a single-chip CMOS device that supports up to 10 full duplex lanes (20 total Rx/Tx pairs) with independent rates up to 28 Gbps for high density line card applications up to terabits per second. The device includes optional support for 802.3bj Clause 91 RS-FEC for 100GE.

### MSH225 DEVICE DESCRIPTION

The flexible, multi-protocol MSH225 PHY device supports a total of 20 independent SerDes lanes with broad data rate capability including 10-15G and 25-28G. For 100GE (4x25G) support, the device includes a 100G RS-FEC specified in 802.3bj Clause 91 for 4x25G NRZ interfaces on lanes 0-3. When the RS-FEC is disabled, the MSH225 device functions as a standard multi-rate and multi-protocol retimer capable of passing data whether encoded or non-encoded.

Each lane is independent and can support a broad range of data rates compatible with 10G, 25G, 40G and 100G Ethernet and OTN standards. With the 100G 802.3bj RS-FEC encode, decode and correction functions enabled, the device will encode data in the B side Tx output direction and decode and correct data (if needed) in the B side Rx input direction. The IEEE 802.3bj RS-FEC enables additional signal integrity and/or distance capability over copper or optical interconnects and has been specified in multiple standards and MSAs including SR4, CWDM4 and PSM4.

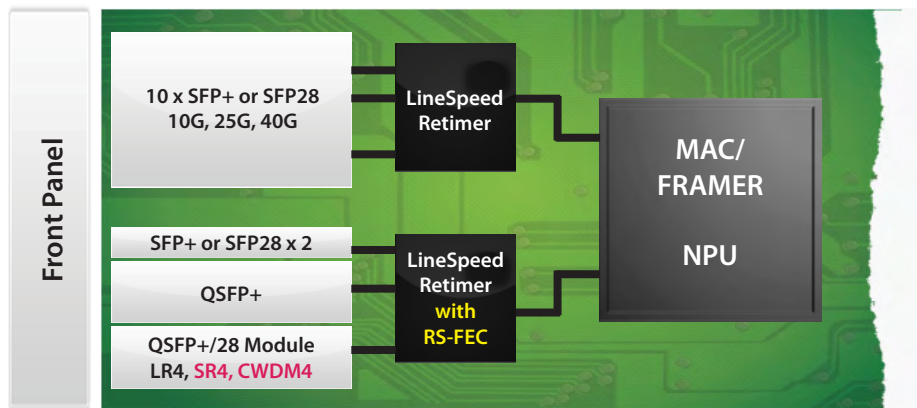
The device is well-suited for supporting signal integrity in high density line cards with mixed protocols and rates.



### FEATURES

- Full duplex 10 lane 28G retimer (20 lanes)
- Support of multiple protocols including IEEE and OIF 10, 25, 40 and 100G standards for Ethernet and OTN
- Optional 802.3bj Clause 91 RS-FEC (4x25.78G) on lane 0-3
  - Specified in SR4, CWDM4, PSM4
- Protocol and rate independent lanes, PLL per lane
- Self-adapting equalizer and eye opening capability
- Integrated Rx 100 ohm termination resistors and AC coupling
- Transmitter and TX pre-emphasis
- Per lane PRBS generator and bit error rate checker
- Flexible power and configuration options
- Reverse polarity control on all inputs and outputs
- Internal registers can be accessed by I2C, MDIO or SPI ports
- Base register configuration and FW provided for ease of use
- Software and register compatible with LineSpeed Flex Devices

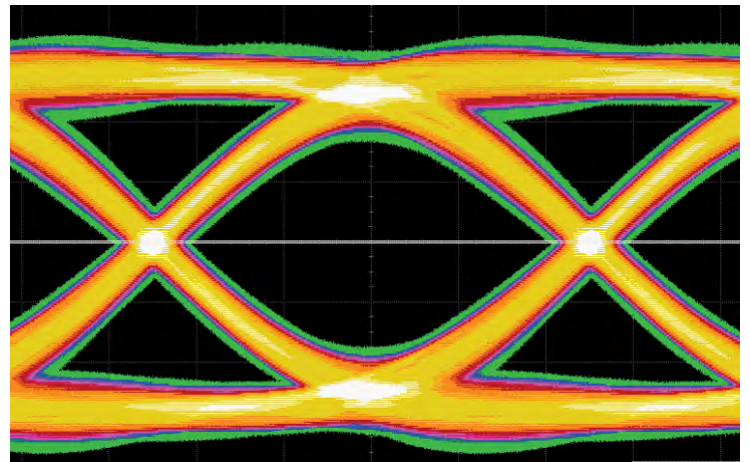
## MSH225 APPLICATION EXAMPLE: Flexible retimer for 10, 25, 40, and 100G interfaces



### MSH225 DEVICE SIGNAL INTEGRITY

To ensure signal integrity, the MSH225 10-Lane Retimer with RS-FEC has the following circuits:

- Opening the eye: A combined analog and digital RX Equalizer
- Retiming: A data slicer plus a clock and data recovery circuit
- Bit stream alignment: Deserializer, frame sync and deskew functions
- Clock synchronization: An elastic buffer for data alignment
- Pre-distortion compensation: A serializer and transmit equalization circuit
- Optional 802.3bj Clause 91 RS-FEC for 4x25NRZ for improved signal integrity
- Diagnostic capabilities to monitor and count correctable and uncorrectable FEC errors



### PACKAGING

- 17mm x 17mm 256 FCBGA (1.0mm)
- Pin compatible with LineSpeed Flex 17mm devices



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