LineSpeed™ Flex MSH222

100G Full-Duplex Retimer with RS-FEC

PRODUCT BRIEF

MSH222 DEVICE OVERVIEW

The MoSys® LineSpeed Flex MSH222 100G Full Duplex Retimer is a single-chip CMOS device supporting up to 4 full duplex lanes with independent rates up to 28 Gbps for high density line card applications in networking, data center and cloud infrastructure. The flexible, multi-protocol SerDes device includes options for 100G RS-FEC.

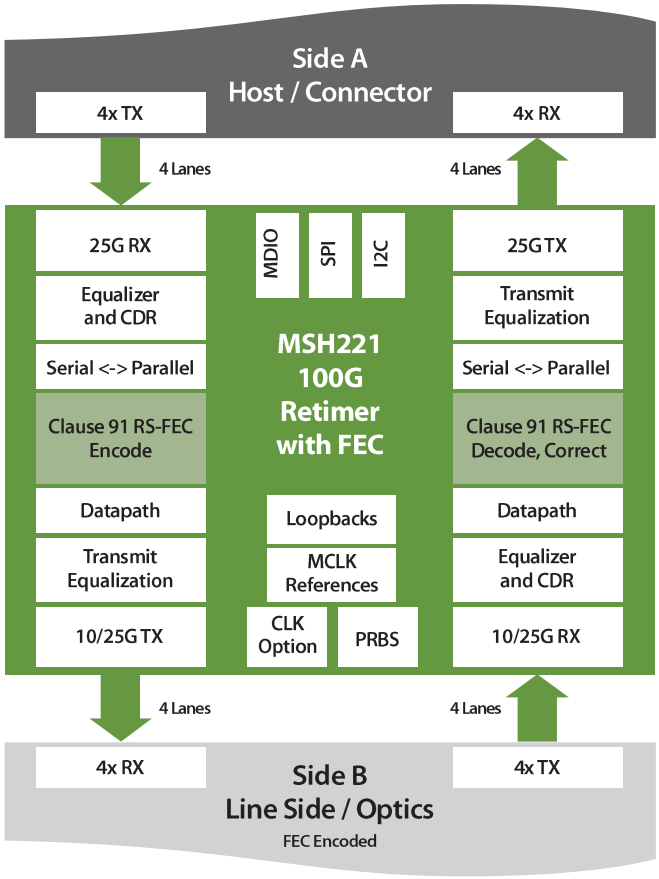
MSH222 DESCRIPTION

The MSH222 is a flexible multi-protocol retimer supporting a wide range of interfaces and rates for applications including high density 10G, 25G, 40G and 100G line interface cards for Ethernet and OTN systems.

When configured as a retimer, the device supports up to 8 channels (4 full duplex) that can be independently configured, retimed and retransmitted. Each multi-rate SerDes lane can support nominal data rates ranges of 10-15G and 25-28G operation.

The MSH222 has two banks of SerDes, referred to as A Side lanes and B Side lanes, connected together by a digital section. Tracing the data path in either direction, the input data goes to an equalizer for opening the eye, a data slicer for digitizing the data, a clock & data recovery block for retiming, a serial to parallel converter, a digital section for data translation, buffering and optional RS-FEC encode (A→B) and decode / correct (B→A) capability, a parallel to serial converter, transmit de-emphasis to add optional pre-cursor and post cursor, and an output driver.

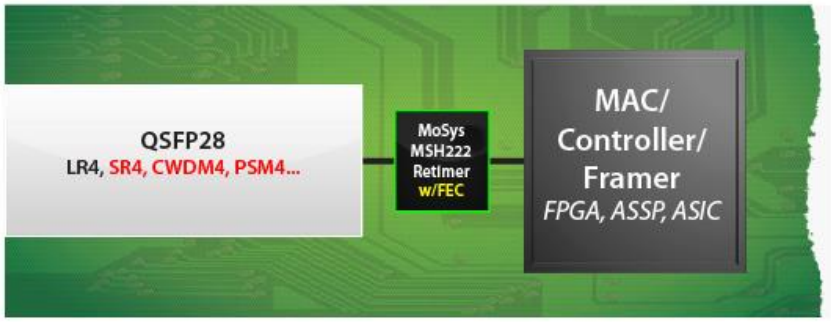
The MSH222 is managed with 16-bit register configuration which can be accessed through three interfaces: (1) I2C, (2) MDIO, or (3) SPI.



FEATURES

- Full duplex 100G 4x25G retimer (8 total lanes)
- Support of multiple protocols including IEEE and OIF 10, 25, 40 and100G standards for Ethernet and OTN
- Optional 802.3bj Clause 91 RS-FEC (4x25.78G)
  - Specified in SR4, CWDM4, PSM4
- Protocol and rate independent lanes with PLL per lane
- Self-adapting equalizer and eye opening capability
- Integrated Rx 100 ohm termination resistors and AC coupling
- Transmitter and TX pre-emphasis
- Per lane PRBS generator and bit error rate checker
- Flexible power and configuration options
- Reverse polarity control on all inputs and outputs
- Internal registers can be accessed by I2C, MDIO or SPI ports
- Base register configuration and FW provided for ease of use
- Software Compatible with LineSpeed Flex PHY family

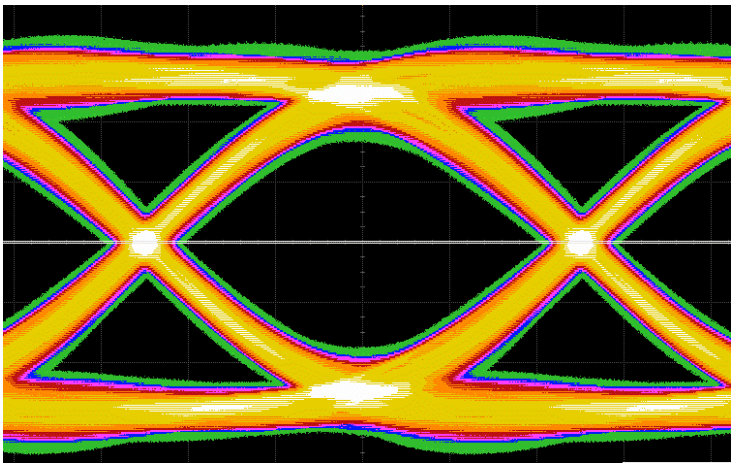
MSH222 APPLICATION EXAMPLE : Flexible retimer for 10, 25, 40 and 100G interfaces



MSH222 DEVICE SIGNAL INTEGRITY

To ensure signal integrity the MSH222 100G Full Duplex Retimer with RS-FEC has the following circuits

- Opening the eye: A combined analog and digital RX equalizer
- Retiming: A data slicer plus a clock and data recovery circuit
- Bit stream alignment: Deserializer, frame sync and deskew functions
- Clock synchronization: An elastic buffer for data alignment
- Pre-distortion compensation: A serializer and transmit equalization circuit
- Optional 802.3bj Clause 91 RS-FEC for 4x25G NRZ for improved signal integrity
- Diagnostic capabilities to monitor and count correctable and uncorrectable FEC errors



PACKAGING

- 13mm x 13mm 144 FCBGA (1.0mm)

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