**MSH221 DEVICE OVERVIEW**

The MoSys® LineSpeed Flex 100G Octal Retimer with integrated RS-FEC (MSH221) is a single-chip CMOS device that can support up to 4 full duplex lanes (8 lanes total) with independent rates up to 28 Gbps for module or daughter card applications. The device includes optional support for 802.3bj Clause 91 KR4 RS-FEC.

**MSH221 DESCRIPTION**

The flexible, multi-protocol MSH221 PHY device supports a total of 8 independent SerDes lanes with data rate flexibility including 10-15G and 25-28G. For 100GE (4x25G) support, the device supports optional RS-FEC specified in 802.3bj Clause 91 for 4x25G NRZ interfaces. When the RS-FEC is turned off, the MSH221 device functions as a standard multi-rate and multi-protocol retimer capable of passing data whether encoded or non-encoded.

Each lane is independent and can support a broad range of frequencies compatible with 10G, 25G, 40G and 100G Ethernet and OTN standards. With the 100G 802.3bj RS-FEC encode, decode and correction functions enabled, the device will encode data from A Side to B Side and decode and correct data (if needed) in the other direction. The IEEE 802.3bj RS-FEC enables additional signal integrity and/or distance capability over optical or copper interconnects and has been specified in multiple standards and MSAs including SR4, CWDM4 and PSM4.

**FEATURES**

- Full duplex 100G retimer (8 lanes)
- Support of IEEE and OIF 10, 25, 40 and 100G standards for Ethernet and OTN
- Includes 802.3bj Clause 91 RS-FEC (4x25.78G)
- Specified in SR4, CWDM4, PSM4
- Independent lane rates
- Self-adapting equalizer and eye opening capability
- Integrated Rx 100 ohm termination resistors and AC coupling
- Transmitter and TX pre-emphasis
- Per lane PRBS generator and bit error rate checker
- Flexible power and configuration options
- Reverse polarity control on all inputs and outputs
- Internal registers can be accessed by I2C, MDIO or SPI ports
- Base register configuration and FW provided for ease of use
- Small 12x12mm package for modules or daughter cards
MSH221 APPLICATION EXAMPLE

MSH221 DEVICE SIGNAL INTEGRITY
To ensure signal integrity the MSH221 100G Octal Retimer with RS-FEC has the following circuits on all 10-28G signal paths:
- Opening the eye: A combined analog and digital RX equalizer
- Retiming: A data slicer plus a clock and data recovery circuit
- Bit stream alignment: Deserializer, frame sync and deskew functions
- Clock synchronization: An elastic buffer for data alignment
- Pre-distortion compensation: A serializer and transmit equalization circuit
- Optional 802.3bj Clause 91 RS-FEC for 4x25G NRZ for improved signal integrity
- Diagnostic capabilities to monitor and count correctable and uncorrectable FEC errors

PACKAGING
- 12mm x 12mm 529 pin FCCSP (0.5mm)