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QUAZAR FAMILY of Integrate Circuits

Memory

*Performance/Cost Target Memories*

**Quad Partition Rate Engine (QPR)**
- QPR4 576Mb memory
- QPR8 1Gb memory
- Low Cost QDR alternative
  - Replace 4 QDRs
  - *For less than $200 in volume*
- Higher bandwidth
  - Up to 240Gb/s
- Lower power
- Pin compatible with BLAZAR family

BLAZAR FAMILY of Integrate Circuits

**Accelerator Engines (AE)**

**Bandwidth Engine (BE)**
- BE2 576Mb memory
- BE3 1Gb memory
- QPR PLUS Acceleration
  - In-Memory Acceleration Functions
  - Two options
    - Burst (12+ functions)
    - RMW with ALU (17+ functions)

**Programmable HyperSpeed Engine (PHE)**
- Same as BE3 (1Gb memory)
- PLUS 32 RISC CPU cores

STELLAR FAMILY of FPGA/ASIC IP

Virtual Accelerator Engines (VAE) - *IP that is Scalable and Portable*
Based on GME (Graph Memory Engine)

LINESPEED Integrated Circuits

**Networking Signal Management**

**Retimers, Gearboxes, Mux/Demux for Line Cards and Modules**

**Gearboxes**
- 100G Gearbox
  - with and without RS-FEC
- 100G Multi-Link Gearbox (MLG)
  - 10 x 10GbE Breakout

**Retimers**
- Protocol Independent Retimer
  - 100G (4x25G) Retimer
    - with and without RS-FEC
  - 10-Lane Full Duplex 25G Retimer

**Mux/Demux**
- 2:1 Serial Multiplexer/Demultiplexer
  - Redundant Link Mode option
We have created new ways to manage traffic flows at lower latencies

- Proven family of FPGA accelerator engine ICs
- New Virtual Accelerator Engine IP to classify packets at line rate
- New performance levels – 100s of gigabits per second
  - Can handle the millions of rules required to manage so many devices
  - Can manage the millions of routes required to route virtual flows
  - Can easily add security through millions of complex Access Control Lists
- All done in parallel, which greatly reduces latency
- Solution based on proven Intel® FPGAs – Easy plug-in solution
MoSys Stellar Packet Classification IP – What Is It?

- Ultra High-Speed Search Engine IP for FPGA
  - Includes advanced TCAM-like compiler (Ternary Content-Addressable Memory)
  - Optimized for Intel® Agilex™ FPGAs and Intel® Stratix® 10 FPGAs
- TCAM-like functions - supports n-tuple Access Control Lists (ACLs) and Longest Prefix Match (LPM)
- Up to multigigabit TCAM equivalence with millions of rules – very wide TCAMs
- Supports a wide range of Internal SRAM and external high-speed memories
- Based on MoSys Graph Memory Engine
- Very fast rule updates - atomic – no need to stop traffic
MoSys Memory & Accelerator Chip Family Overview

Communications/ Packet Processors, SmartNIC, SmartSwitch, SmartStorage…

FPGA

• 576Mb and 1Gb High-Speed Memory
• Extends Packet Classification Platform Capacity
• Offloads FPGA
• Very Low Latency & Power Efficient
• Low Pin Count
  • Serial Attachment but looks like QDR memory inside the FPGA
  • Optional RISC engine accelerators

Optional Accelerators

RISC Processor Engines

576Mb or 1Gb memory

SerDes

Rx

Tx

SerDes

Arithmetic

Statistics

QDR-like interface

Add high performance memory to FPGA for even more rule capacity
MoSys Broad Family of Memories & Accelerators

Flexible Intelligence

- Lookup & Fast Buffer
- Statistics & Metering
- QDR-like Memory

- 12.5G / 576Mb
- 25G / 1Gb

- Programmable HyperSpeed Engine
- Accelerators

- PHE
- Blazar Bandwidth Engine - Accelerators
- Blazar BE3
- Blazar BE2

- Quazar Quad Partition Rate (QPR) Memory
- Quazar QPR8
- Quazar QPR4

PHE includes 32 RISC cores (256 vcores)
Further Extends Search Performance & Offloads FPGA
Blazar & Quazar – Three Typical Silicon Use Cases

Delivers Highest Performance

• Highest Efficiency Interface Protocol
• Up to 480 Gbps I/O bandwidth
• 32 concurrent memory ops
• Stats include aging activity bits
• Highest Look-Up Performance ➢ up to 5+ billion reads per second

1) Blazar Adds Stats & Metering – Up to 32 x 100G

2) Blazar & Quazar Buffer - Up to 400G Full Duplex

3) Blazar & Quazar Packet Classification Platform - Table Lookup Up to 5B Read/s

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1st Polling Question

- Q1) Do you have high bandwidth FPGA applications (80Gbps or above aggregate line rates)?
  - I design 80Gbps or above aggregate line rate boards
  - I am considering using TCAMs
  - My application includes Packet Header Inspection, Payload inspection, Look Up Tables
  - My application may need small (5-10ms) ingress or egress smoothing buffers
Accelerator Engine
Performance Based on Architecture

QPR4/8
Memory Ops:
Rd/Wr 72b
Wr 36b

BE2/3 BURST
In Memory Functions
8/16 Reads
8/16 Writes

BE3 - Double the Read & Write capability

Partition
Banks

Results

GCI-A
GCI-B

10-25G Rx SerDes
10-25G Tx SerDes

BE2:
576Mb, 4 Partitions, 64 Banks
BE3:
1.1Gb, 4 Partitions, 128 Banks

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MSR 622/820/630/830 Single Chip Buffering:
Full Duplex Data Throughput

- **Effective throughput of payload; 72b per word**
  - BL# = Burst length; linear burst of 2, 4 or 8 words
- **Full duplex: balanced read and write**

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<th>Throughput (Gbps)</th>
<th>Speed Grade</th>
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<tr>
<td></td>
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<tr>
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<td>29.7</td>
</tr>
<tr>
<td>BL2</td>
<td>24.8</td>
</tr>
</tbody>
</table>

**Sigma Quad IVe BL4 is:**
- 93 Gbps Full Duplex (192 Gbps I/O throughput)
- 8 x 16Mb single ported banks
- ~4.5W (device + I/O)

**QDR IV XP is:**
- 76.5 Gbps Full Duplex (153 Gbps I/O throughput)
- 8 x 16Mb single ported banks
- ~7W (device + I/O)

**RLDRAM 3:**
- 33 Gbps Full Duplex (76.5 Gbps I/O throughput)
- 8 x 16Mb single ported banks
- ~3.5W (device + I/O)
Pipelining With BE3 As A Dual Port
Memory Architecture is Critical
Increase Performance AND Save Space/Cost

Parallel vs Serial

QDR (Memory Competitor) Parallel Connection

QDR  QDR  QDR  QDR

536 - 720 SIGNALS

FPGA

Memory 576Mb

QPR BE2

MoSys Bandwidth Memory Serial Connection

QDR  QDR  QDR  QDR

1072 - 1440 SIGNALS

FPGA

Memory 1Gb

QPR BE3

Space & Cost Considerations

Performance Balance of Memory vs Space

• Space and Memory Capacity
  • One QPR/BE2 = 4 QDR … 512Mb
  • One QPR/BE3 = 8 QDR … 1Gb

• Part Cost
  • 1-QPR/BE2 for 576Mb memory ~ 2x cost of one QDR
    • 4x Memory
  • 1-QPR/BE3 for 1Gb memory ~ 2.5x cost of one QDR
    • 8x Memory

• Design time
  • Reduces signal routing time and layout
  • Told it saved 6-9 months

• Signal Integrity
  • Comparable QDR system has 536-1440 clean signals generally requiring external components
  • MoSys system typical has 32 signals with on board Auto-Adaptation signal tuning
    • No external components

• Power
  • ~ Half

• Bandwidth
  • Random data access is equivalent (tRC 2.7-3.2 ns)
  • For certain applications, much faster
3rd Gen Memory Architecture
16 Dual Counter ALUs ➔ 5B RMW Ops/s

Round Robin Scheduler

8 Operations per partition per clock ➔ 32 Total

2.67ns tRC ➔ 250 to 375 MHz:
16 Reads
16 Writes ➔ Up to 5BA/s

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Programmable HyperSpeed Engine (PHE) Architecture

❖ Physical
  ▪ 16 x 10 to 30Gbps PHY
  ▪ SerDes Standard GigaChip Interface (GCI) Protocol
  ▪ 8 Scheduling Domains
  ▪ Integrated 1Gb Fast Memory

❖ Threaded Processor Engines
  ▪ 32 cores (8 clusters of 4 PE)
  ▪ Up to 1.5GHz
  ▪ 8 threads per PE
  ▪ Search-optimized ISA

❖ Internal Performance
  ▪ 5B Rd/s + 5B Wr/s
  ▪ 3ns tRC
  ▪ Access up to 144 bits/cycle

❖ 676 FCBGA 27x27mm, 1mm
Instruction Set Overview

- **ALU/Logical on 72b**
  - add, sub, adc, sbb, s1add, s2add, s3add, s3sub, and, or, xor, andn, sar, slr, sll, minu, maxu, mult
- **Bit field of variable len @ variable pos**
  - Extract, deposit, chomp
  - Can be across register boundaries
  - Optional auto incr of pos
- **Special Functions**
  - Find first zero, find first one
  - Population count
  - Swap bits in bytes and bytes in words
  - 144b HASH to 72b (non-crypto)
  - Compute CRC32
  - Multi-way compare with 4, 6, 9 & 12 inputs
- **Test & Branch**
  - tsteq, tstgt, tstnle, tstlt, tstnge, tstgtu, tstnleu, tslltu, tstngeu, tsllbs, tslnue, tsntle, tsntleu, tsntgt, tsntge, tsntlnt, tsntleu, tsntngtu, tsntgeu, tsntntu, or tsntbc
  - Jmp, jeq, jgt, jnle, jlt, jnge, jgtu, jnleu, jltu, jngeu, jbs, jne, jle, jngt, jge, jnlt, jleu, jngtu, jgeu, jnltu, or jbtc
  - Multiway branch 2, 3 & 4
- **Loads & Stores**
  - Local Dmem:
    - 8, 16, 32, 64 & 72b
    - Reg + offset, w/auto incr reg
  - Partition:
    - Burst reads, load balanced reads and broadcast
    - 64, 72, 128, 135, 144b
    - Reg + reg or reg + offset, w/auto incr reg
- **Atomic Operations**
  - Local:
    - 8, 16, 32 & 64b
    - adda, suba, anda, xora, andna, xchga, cmpxchga
  - Partition:
    - 16, 32, & 64b
    - Add(s), sub(s), xor, rd/set, tst/set, cmp/set, avg, tm, age
- **Program Control**
  - Hlt, Brk & nop
  - Add/mov & halt (tread)
  - Yield
- **Special registers**
  - GPR indirect specification
  - Auto increment
  - Command, memory, result, result len
  - Time stamp, random, zero, all ones, thread id, wake up, sink
Summary

- Bandwidth Engine 2 and 3 in full production
- Over 200K shipped, no field failures
- Qualified as Enterprise Grade and ships to some of the largest networking and security companies in the world
- Replaces between 4 and 8 QDR devices
- Price savings
- Board design time savings
- Proven interop with Intel and Xilinx FPGA devices
- Eval boards available
- MoSys supports custom controller development for customers
- Available in Commercial and Extended temp
  - 0C to 85C
  - 0C to 100C
- Bandwidth Engine 3 is available in Industrial Temp
  - -40 to 85C
Q2) Are you working on a 5G design?

- Yes in the next 6 months using a custom design
- Yes in the next 6 months designing to a Service Provider spec
- Yes in the next 12 months using a custom design
- Yes in the next 12 months designing to a Service Provider spec
- No not working on a 5G specific solution
MoSys Stellar
Packet Classification Platform
Overview – Non-NDA

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Stellar Packet Classifier Platform Exec Summary

- **Ultra High-Speed Search Engine IP** for ASIC/FPGA plus advanced TCAM-like compiler
- **TCAM-like functions** - supports n-tuple ACLs & LPM
- **Can be optimized to work with a wide range of High-Speed Memories**
  - ASIC SRAM, FPGA M20K, eSRAM, BRAM, URAM, DDR4, HBM and/or other external memory
- **Graph Memory Engine** – Allows easy mapping of complex rules
- **Very fast updates** - can be dynamically updated on the fly – incremental or full updates
- **Flexible** – ASIC/FPGA only or ASIC/FPGA plus external memory i.e. MoSys memory or HBM
- **Performance**
  - **Up to multigigabit TCAM** equivalence with **millions of rules**
    - can greatly extend internal Switch and SmartNIC TCAM functions
  - **Hundreds of Millions searches per second**
  - **Hundred of Gigabits per second**
Why MoSys? How Do We Solve the Pain?

We have created new ways to manage traffic flows at lower latencies

• Proven family of FPGA accelerator engine ICs
• New Virtual Accelerator Engine IP to classify packets at line rate
• New performance levels – 100s of gigabits per second
  • Can handle the millions of rules required to manage so many devices
  • Can manage the millions of routes required to route virtual flows
  • Can easily add security through millions of complex Access Control Lists
• All done in parallel, which greatly reduces latency
• Solution based on proven Intel® FPGAs – Easy plug-in solution
5G Core & Edge Use Cases – UPF Locations

- UPF appears in 2 places
  1) Core Network
  2) At the Edge inside a MEC (Multi-Access Edge Controller)

- Often based largely on SmartNIC or SmartSwitch as software only cannot handle required performance

- Control info comes for SMF using Packet Forwarding Control Protocol (PFCP)

- SMF acts as a sort of SDN Controller

- UPF can contain millions of rules
  - Non learned
  - All come from SMF

---

Simplified diagram (not all connections shown)
Packet Processing Architecture MoSys Stellar IP

Management / Control Plane over PCIe from x86

Parser Engine

Match-Action Engine

Deparser Engine

PHY

PHY

P4 Programmable IP shown by blue line

MoSys LPM and ACL engine IP shown by green line

MoSys LPM and ACL Match Lookup Engine

Intel® Stratix®10 FPGA with high bandwidth memory
MoSys Stellar Packet Classification Platform

Two main IP product lines both take advantage of our Scalable Graph Memory Engines (GME)

1) **High Flexibility / High Complexity ACL & LPM IP**
   - Up to 200 Gbps at 300 MHz FPGA*
   - 1 – 10+ tuple, 40 - 480b typical key size
   - ACL rules up to 16+ million
   - Up to 150 million lookups per second

2) **High Performance / High Capacity LPM IP**
   - Up to 400 Gbps at 300 MHz FPGA*
   - 1 – 2 tuple, 40 - 160b typical key size
   - LPM rules up to 4+ million
   - Up to 300 million lookups per second

**GME Scalable Performance**
- Performance is scalable to meet your rule and lookups/sec requirements
- Multiple Graph Memory Engines (GME) can be combined for other configurations
- Parameterizable to optimize for bandwidth, lookup rates, number of rules or logic/memory usage

**Licensing Model** – One time license plus per use royalty, annual maintenance

---

**Choose 1 for higher complexity**
**Choose 2 for higher performance**

---

*up to 3X with ASIC at 900 MHz
Subject to change
3rd Polling Question

Q3) In your 5G application do you need Packet Classification IP for your FPGA?

- I would prefer to use FPGA RTL IP and on chip SRAM and/or external DRAM to do Packet Classification and Search vs. external TCAMs
- I will implement Exact Match, LPM and/or ACLs
- I need to use HBM already so Packet Classification IP that can leverage this would be valuable
- I will implement Security functions like Firewalls, Anti-DDoS
Stellar Scalable Performance – 1x to 100x+ Range

- MoSys Packet Classification Platform can run on variety of Graph Memory Engines (GME)
  Available as Software, FPFA/ASIC RTL or Firmware for PHE

- Scalable across many platforms
  - From “C” → ASIC/FPGA IP core + Internal SRAM and optional DDR/HBM/MoSys BE2/BE3/PHE memories → RISC cores
  - Same high-level software interface across all platforms
  - Memory allocation is transparent to SW - eases porting

Software
1X per core

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<th>Customer Code</th>
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10X/30X

- FPGA/ASIC
- Customer RTL
- GME IF
- GME RTL
- Internal SRAM

20X/60X

- FPGA/ASIC
- Customer RTL
- GME IF
- GME RTL
- Internal SRAM

40X/120X

- FPGA/ASIC
- Customer RTL
- GME IF
- GME RTL
- Internal SRAM

100X per PHE

- FPGA/ASIC
- Customer RTL
- GME IF
- GCI/Serdes

Optional DDR or HBM or MoSys memories to increase rule capacity

Assumes FPGA at 300MHz/ASIC at 900MHz

MoSys PHE

GME on RISC
1Gb SRAM

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MoSys Graph Memory Engine (GME)

- GME uses graph to inspect packet header

Sample set of TCAM style rules
1, 0 and * (don’t care)
MoSys Multi-Field Multi Match Example

Test rule 100 @ tcam entry 100

Cycle 0
k[0x00000000] <HashNode0> -> p[0/8] <HashNode 1> @ depth 0
[10101100 00010111 00000100 11110110 10001001 10101011 01010010 11010100]

Cycle 1
10101100[0x000000ac] --> k[0x00000000] <HashNode1> --> p[32/8] <HashNode 5959 >
[10101100 00010111 00000100 11110110 10001001 10101011 01010010 11010100]

Cycle 2
10001001[0x00000089] --> k[0x00000000] <HashNode59 > --> p[40/16] <HashNode 59>
[10101100 00010111 00000100 11110110 10001001 10101011 01010010 11010100]

Cycle 3
* --> k[0x00000000] <HashNode6175 > --> p[8/16] <HashNode 6176 > @ depth 6
[10101100 00010111 00000100 11110110 10001001 10101011 01010010 11010100]

Can have multiple rules that match
Stellar IP sorts out which is the best match based on rule priority
Thank You

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LineSpeed™ 100G PHY IC Family

Flexible Line Card & Module Solutions
LineSpeed™ 100G PHY ICs

Applications

- Extending Reach of High-Speed Serial Links
  - Retimers with up to 20 lanes at 28Gb/s
- QSFP28-based Optical Interfaces
  - 100G (4x25G) Retimer w/ and w/o RS-FEC
  - 100G Gearbox w/ and w/o RS-FEC
- Bringing High-Speed Links to low-cost FPGAs
  - Mux/Demux of low-speed I/Os into high-speed I/Os
- Breakout of 100G ports to 10 x 10Gb Ethernet
  - Multi-Link Gearbox (MLG), including SyncE support
- High-Availability Systems with Redundant Links

Key Features

- Family of Retimer, Gearbox, & Mux/Demux ICs
- Compliant to IEEE, ITU, and OIF standards
- 100G RS-FEC encoder/decoder (optional)
- Redundant Link Mode for Protection Switching
- Independent baud rates per lane
- Strong, self-adapting receive equalizers
- Built-in PRBS generation and checking
- Multiple packages for line cards and modules
- **Priced at less than $50 in volume**

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<th>Description</th>
<th>TX/RX Lanes</th>
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<th>Gearbox</th>
<th>MLG</th>
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# Accelerator Engine Devices

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<tr>
<th>In-Memory</th>
<th>Part Number</th>
<th>Description</th>
<th>Package</th>
<th>Interface</th>
<th>Memory</th>
<th>Access Rate</th>
<th>In-Memory Functions</th>
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<tr>
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<td>Pkg Size</td>
<td>Lane</td>
<td>Rate per Lane Gb/s</td>
<td>BW MAX.</td>
<td>IRC</td>
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Thank You