MoSys High-Speed Board Design Guidelines

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Topics

- Intro to MoSys
- Terminology
- Impedance **control** layout guidelines
- Crosstalk
- Layout of SerDes traces
- Power integrity

Component overview cross-section of devices and PCB board.

Accelerator Engines & Linespeed Product Lines

QUAZAR FAMILY of Integrate Circuits

Memory

Performance/Cost Target Memories

Quad Partition Rate Engine (QPR)

QPR4 576Mb memory
QPR8 1Gb memory

Low Cost QDR alternative
- Replace 4 QDRs
- **For less than $200 in volume**

Higher bandwidth
- Up to 240Gb/s

Lower power

Pin compatible with BLAZAR family

BLAZAR FAMILY of Integrate Circuits

Accelerator Engines (AE)

Memories with Embedded Acceleration Engines

Bandwidth Engine (BE)

BE2 576Mb memory
BE3 1Gb memory

QPR **PLUS** Acceleration
In-Memory Acceleration Functions
Two options
- Burst (12+ functions)
- RMW with ALU (17+ functions)

Programmable HyperSpeed Engine (PHE)
- Same as BE3 with 1Gb memory
- **PLUS** 32 RISC CPU cores

LINESPEED Integrated Circuits

Networking Signal Management

Retimers/Gearbox/MLG Gearbox

Gearbox

100G Gearbox
- with or without FEC

100G Multi-Link Gearbox (MLG)
- 14 or 20 TX/RX
- for Modules or Line Cards

100G Gearbox with RS-FEC

Retimers/Repeater

Protocol Independent Retimer
100G Octal Retimer with RS-FEC
100G Full Duplex Retimer
- with or without RS-FEC

10 Lane Full Duplex 25G Retimer
- with or without FEC

STELLAR FAMILY of FPGA/ASIC IP

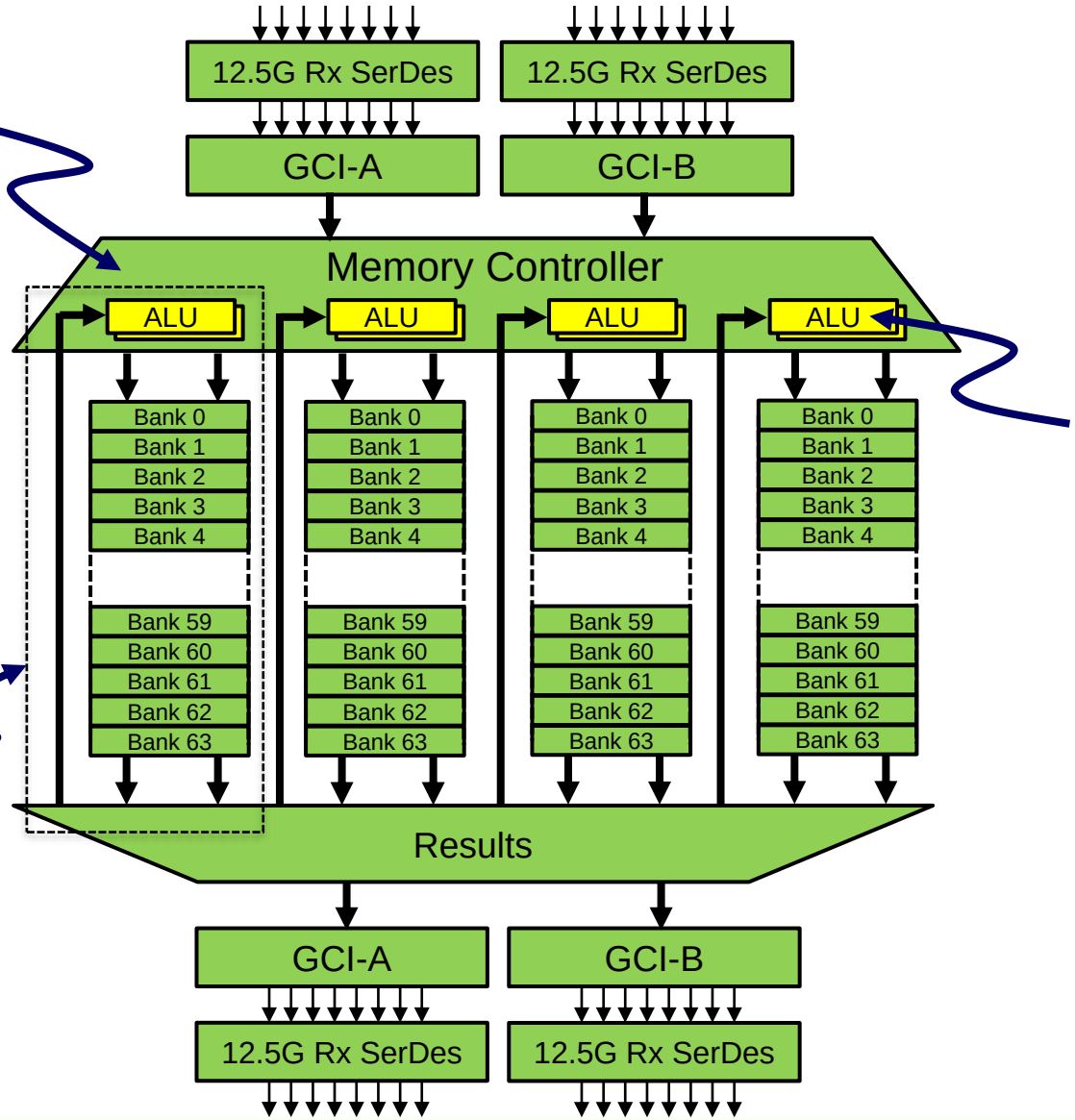
Virtual Accelerator Engines (VAE**) -** ***IP that is Scalable and Portable***
Based on GME (Graph Memory Engine) **Packet Classification Platform**

Bandwidth Engine 2 Architecture

Memory Ops:
Rd/Wr 72b
Wr 36b
Burst Rd/Wr

375 MHz:
8 Reads
8 Writes

Partition

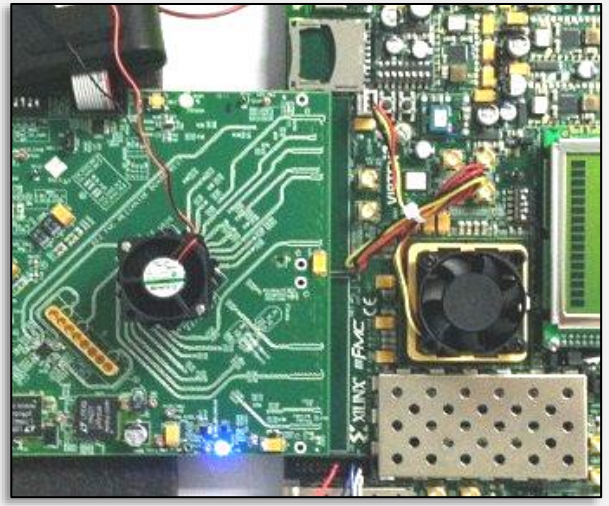


MSR 820
RMW Macro Ops:
Incr/Decr
Dual Incr
Metering
Test & Set
Read & Set

Proven FPGA Ecosystem

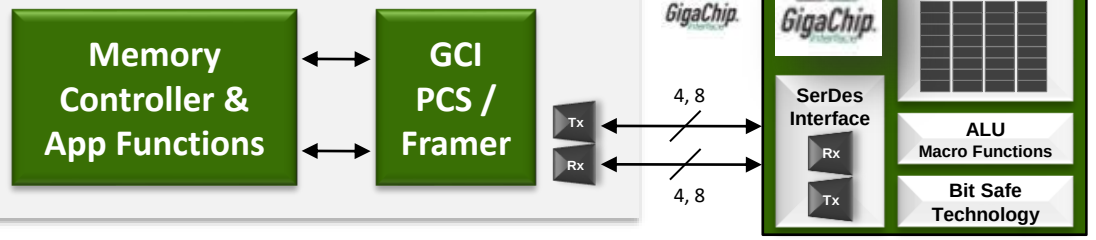
Proven Platforms and Ecosystem with Xilinx and Altera/Intel FPGAs

Intel® Stratix® IV, Stratix V, Arria® 10, Stratix 10



Xilinx® Virtex® -6, Virtex-7, UltraScale™, UltraScale+™

MoSys Provides Reference Designs to Speed Customer Design Process

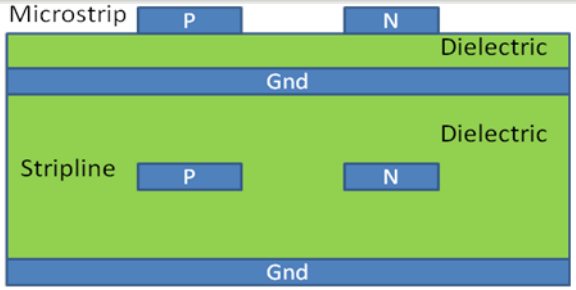


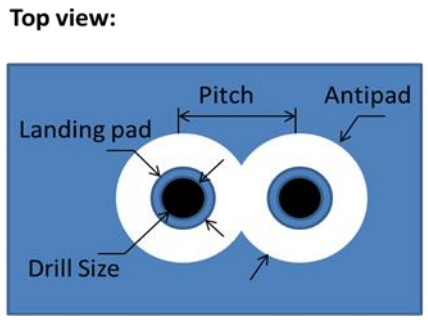
Polling Questions (1)

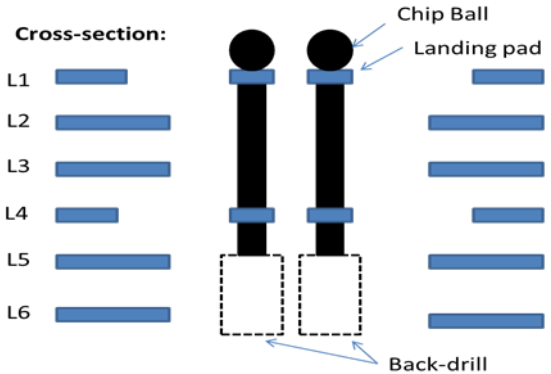
- **Do the designs you are doing utilize SerDes?**
  - A) No
  - B) Yes 10GHz – 15GHz
  - C) Yes 20GHz – 28GHz
  - D) Yes, greater than 28GHz (56GHz - 112GHz)

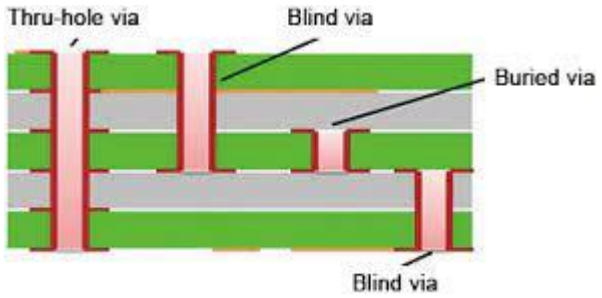
Terminology

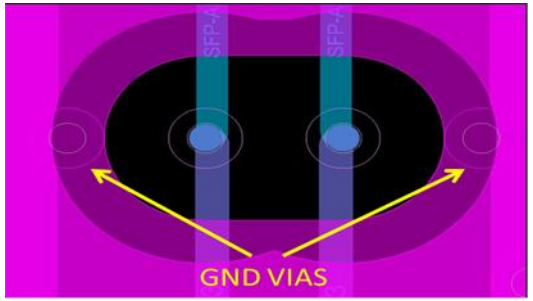
- **Terminology**
  - Microstrip
  - Stripline
- **Via’s**
  - Pitch
  - Landing Pad
  - Antipad
  - Drill Size
  - Stack up
  - Back-drill











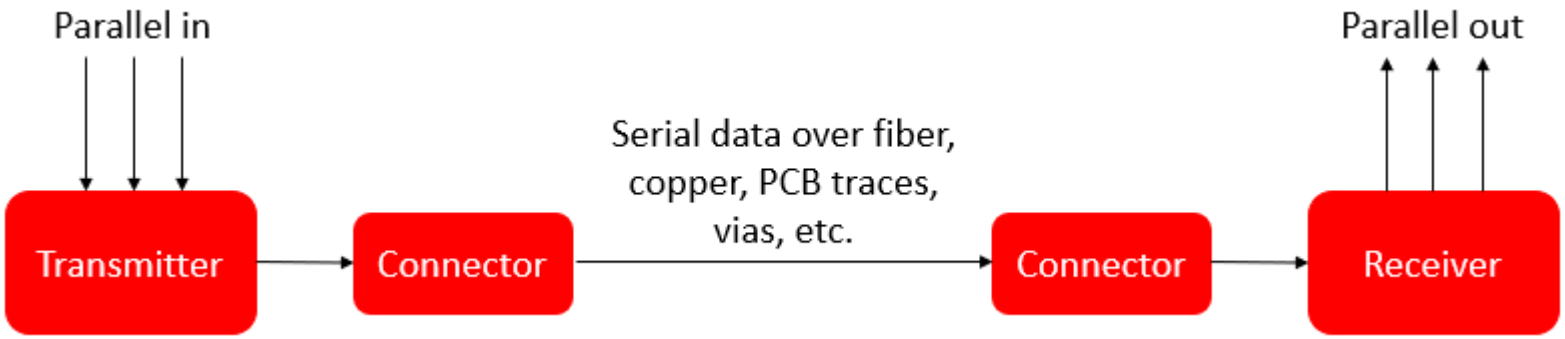
- Selection of PCB Materials, Number of Layers, Speed of connections, PCB design all contribute to a successful design

Terminology

- **Insertion Loss - insertion loss** is the **loss** of signal power resulting from the **insertion** of a device in a transmission line (**Insertion loss** is the ratio of the output signal to the input signal, and it is **measured** in decibels (dB))
- **Return Loss** - **return loss** is a measure in relative terms of the power of the signal reflected by a discontinuity in a transmission line
  - This discontinuity can be caused by a mismatch between the termination or load connected to the line and the characteristic impedance of the line.
- **S-Parameters**. **S** (**scattering**) **parameters** are used to characterize electrical networks using matched impedances.
  - Here, **scattering** refers to the way traveling currents or voltages are affected when they meet a discontinuity in a transmission line.
- An important performance **measure** of a 2-port network is **S21** (Insertion Loss)
  - An S-parameter indicates the amount of power leaving one port of the network, given power entering another (or the same) port of the network.
  - In the case of **S21**, the suffix “21” denotes the power leaving port 2, with power delivered to port 1

Channel

Channel



- **Cross-talk** - Unwanted transfer of signals between communication channels
  - The common electrical interface spec cross talk noise as a function of insertion loss (CEI Spec, 2014)

PCB Material Selection

- Select the material with the lower loss to reduce signal attenuation from dielectric losses.
- Always choose lower Ɛr (dielectric constant) with a flat frequency response for best signal performance and to reduce signal dispersion that adds phase jitter
- Always choose more densely woven fiberglass style for the core and prepreg material surrounding the high-speed signal layers for more uniform Ɛr that will minimize impedance and signal variations
- Choose less dense fiberglass styles for power layers and slower general-purpose signal layers to reduce PCB cost
- Use wider traces and choose rolled copper foils over traditional electrodeposited (ED) copper foils in the PCB construction to mitigate conductor loss

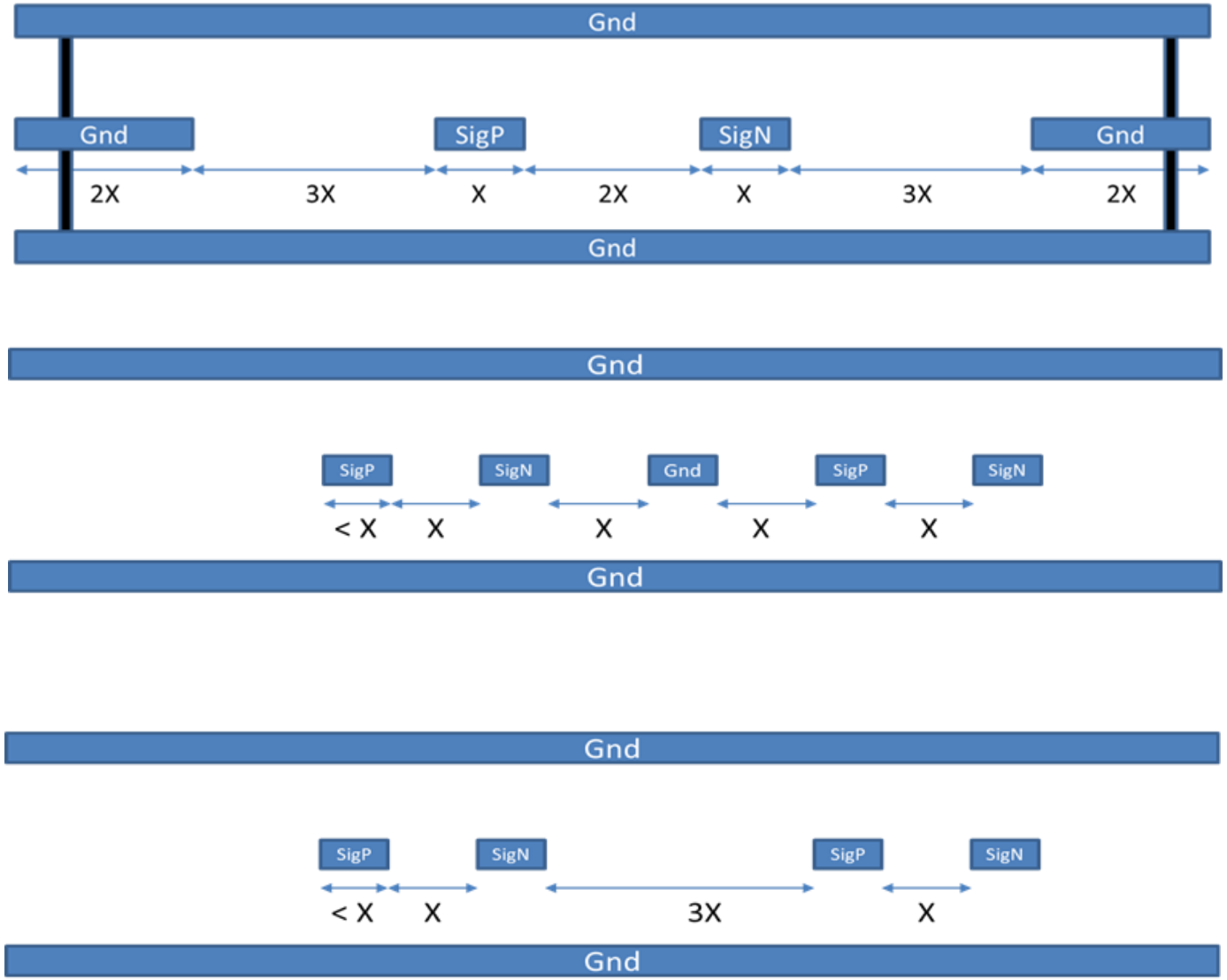
General Issue

- **Nelco 4000-13EPSI**
- **Rogers 4350B**
- **Panasonic Megtron 6**

- **PCBs are becoming very constrained and using fine trace widths down to 4 mils wide to improve routability.**
  - For high-speed signals, narrow trace geometries increases conductor loss
  - Larger signal attenuation occurs for signals at 4 mils vs. 5 to 6 mils.
  - For example, for a 28-Gbps signal, the difference in attenuation at the Nyquist frequency (14 GHz) is approximately 3 dB for 4 mils versus 6 mils wide trace.
  - designers are often forced to use differential signaling to achieve acceptable signal integrity

- **Successful data transmission across these types of links requires the design to minimize signal degradation caused by the channel**

Differential Routing



Ideal

Non-Ideal

Risky

Routing

Ideal

- Used wherever possible
- Safest to keep signal separation and pair Gnd shielding
- Wider trace also easier to maintain desired impedance
- Easier to support smooth gradual turns

Non-Ideal

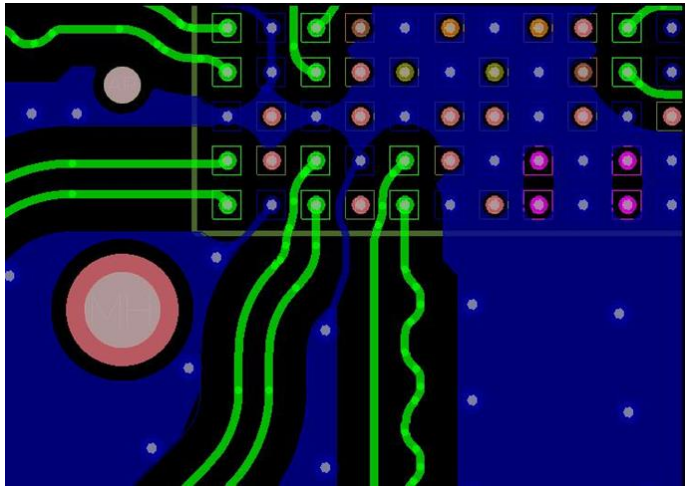
- Used when PCB gets congested
- Often used in breakout region

Risky

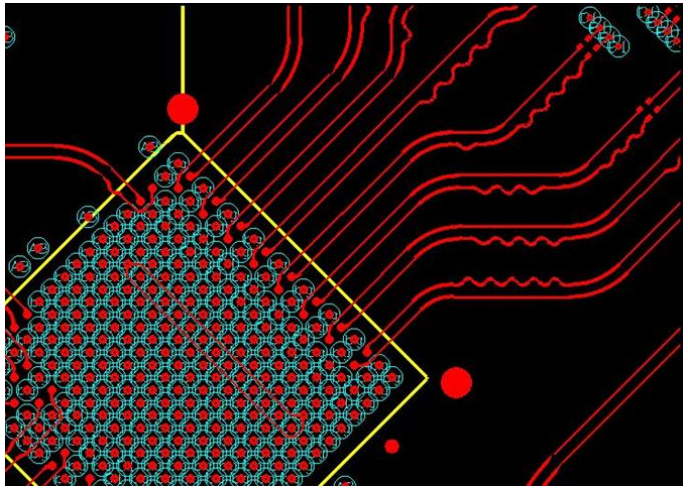
- Used when PCB is Very Congested
- Used in lower frequency Interfaces (Few GHz)

Trace Examples

Ideal



Non-Ideal



Risky
(No Gnd)

Polling Questions(2)

- **Has the use of SerDes been related to large packet transfer functions like Ethernet TCP/IP, FTP, MDP, etc.) or protocols like Interlaken?**
  - A) Packet Transfer
  - B) Chip to Chip

Via's

- **Via Design**

- **The characteristic impedance of differential vias are lower than 100 Ω.**

- **You can minimize C_{via} using the following techniques:**
  - Reduce the via capture or landing pad pad size
  - Eliminate all non-functional pads (NFP)
  - Increase the via anti-pad size to 40 or 50 mils

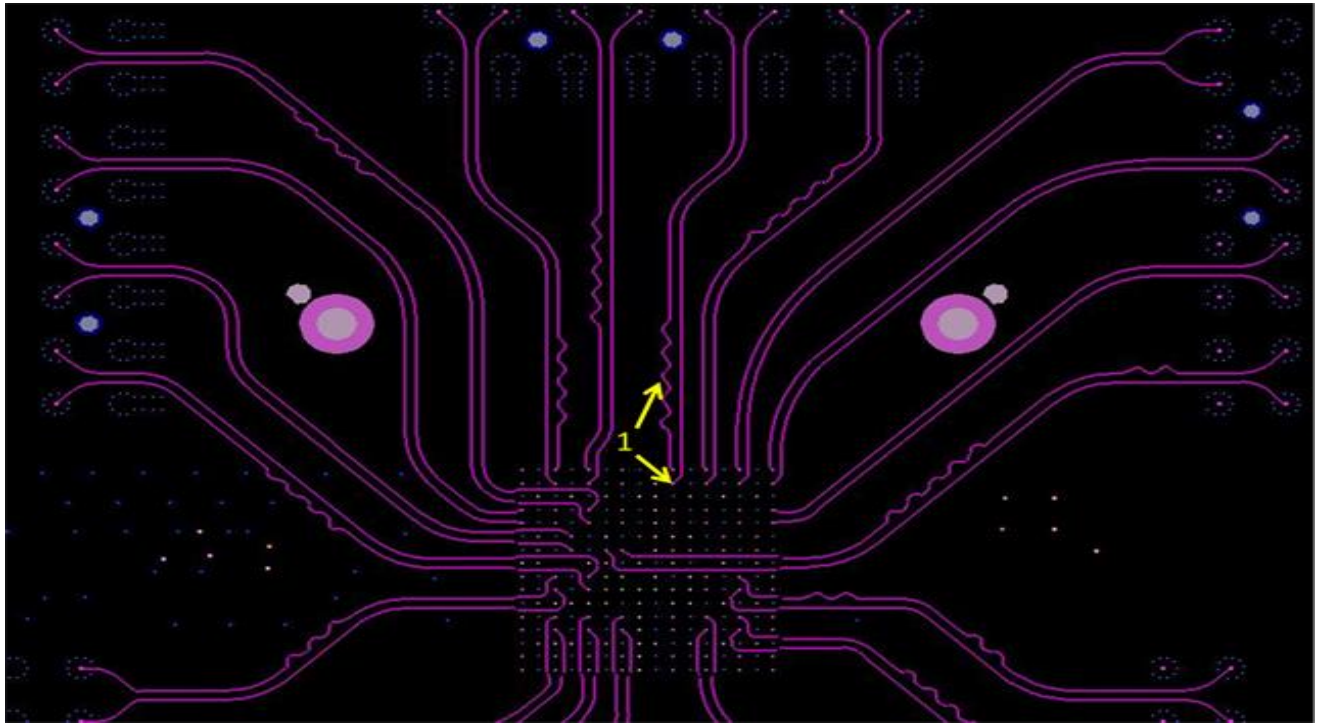
- **You can minimize L_{via} using the following techniques:**
  - Eliminate and / or reduce via stubs
  - Minimize via barrel length by routing the stripline traces near the top surface layer and applying backdrilling

Skew between P and N

- **For a differential pair, positive (P) and negative (N) lines are ideally exactly the same**
  - Not as critical to length and matched/mirror routing all the way from TX to RX.
  - In reality, there will be a difference, physically as well as electrically, for example MoSys devices place Tx and RX on opposite sides of the die
  - A skew between P and N causes a reduced eye margin and a finite common mode signal (differential to common mode conversion).
  - Even with a perfectly match length between P and N, the non-uniform material properties of a PCB could affect the signal delay
  - It is therefore critical to match the lengths accurately in the layout.
  - Data rates of 10-28 Gbps, NRZ, matching lengths within ± 1 mil is recommended

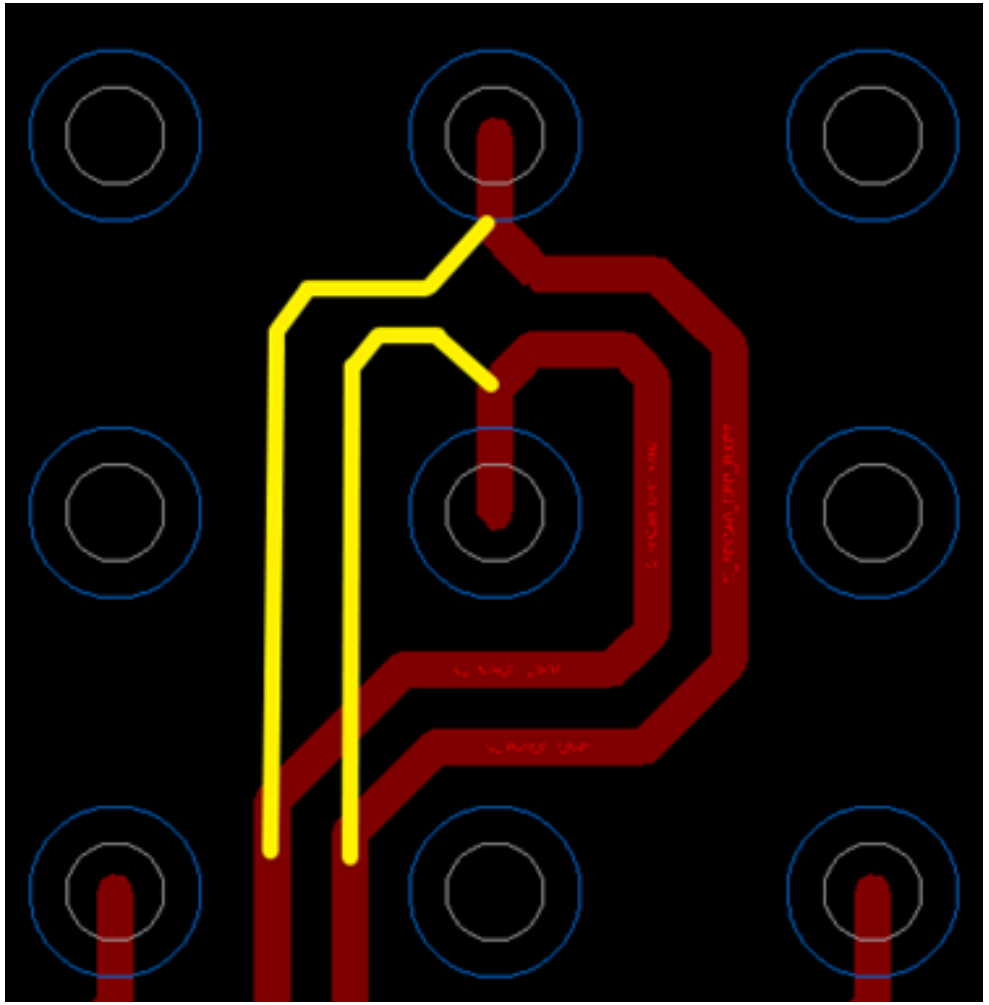
Trace Matching

- The figure below has a length mismatch due to the ballout at the device
- The wiggle pattern is used to increase the length of the shortest trace
- As close to the original mismatch as possible
- The trace to the right of #1 has the length equalization mid-way



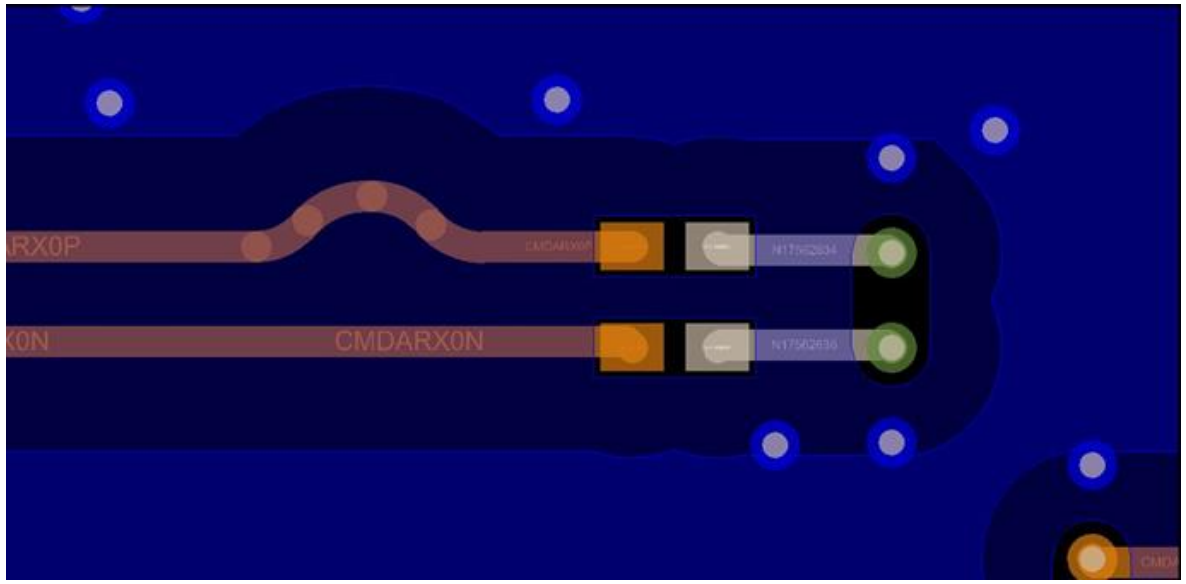
Reverse polarity to optimize layout

- **Polarity of the differential pair can be reversed for both transmitter and receiver**
- **TXP from the host can go to RXN**
- **And TXN to RXP, as the design can internally correct for the polarity**
- **This feature gives freedom to a layout engineer to:**
  - reduce length,
  - simplify routing, and
  - possibly more accurately match trace length



AC coupling capacitor

- **AC coupling capacitors are sometimes required for high-speed signals**
- **Choose an AC coupling capacitor that has a size that is about the same width as the traces**
- **Make the characteristic impedance of the components match as closely to the signal impedance**
- **Illustrated below where 0201 size 0.1µF capacitors**
- **Are slightly wider than the traces and would cause a capacitive discontinuity.**
  - To compensate for this, the ground plane underneath the component is partially cut out
  - This is not ideal, as it makes the ground return not uniform



Power Integrity

- **To reduce supply ripple voltage, it is generally recommended to use power planes in the PCB with alternating VDD/GND layers**
- **Place capacitors as close to the device as possible**
  - Minimize inductance in the PCB traces that connect to the capacitor
  - Treat the supply, the GND as well as parallel path of decoupling capacitors as a continuous plane
- **Place VDD and VSS vias adjacent as pairs to minimize inductance**

- **Di/Dt supply information is not always available.**
  - It is generally recommended to use a range of decoupling capacitors to reduce the ESR over a wide frequency range – e.g. capacitors at 100, 10, 1, and 0.1μF.

Power Integrity Check

- Bulk Decaps - The quantity and values need to be sufficient for supplying lower frequency supply variations
- Decap-Mid and High freq – The quantity and values need to supply higher frequency supply variations
- Tantalum Caps Polarity visible and properly connected
- Check if Caps have sufficient Voltage rating: generally, recommend >2.5X voltage rating
- Check if Ferrite bead used when a power supply is shared between analog and digital domain
- Check if Ferrite bead DC resistance is low such that the power supply voltage level is within tolerance
- Check if Ferrite bead chosen have sufficient current rating
- Make sure Sense line connected very close to the load

Polling Questions (3)

- **Are you directly responsible for PCB design or is it out-source to a PCB design house?**
  - A) I am directly responsible
  - B) I am responsible for providing guidance to a PCB Design house

First order considerations

- **Signal attenuation**
  - Routability must be properly balanced with trace width selection for better performance.

- **Impedance control and discontinuities**

- **Crosstalk**
  - Crosstalk control usually involves reducing signal edge rates and maintaining enough trace-to-trace separation to reduce the mutual capacitive and mutual inductive coupling energy.
    - Reducing the signal edge rate is usually not an option
    - Crosstalk control for high-speed transceiver designs is mainly determined by PCB layout spacing constraints to keep the transceiver traces far enough apart to minimize the coupling effect
    - For very high-speed traces, it is desirable to keep the coupling noise to less than 1% of the source signal

    - Microstrip routing requires a separation of 6H and 7H to properly manage the crosstalk coupling to less than 1%
    - Stripline routing requires only 5H separation to achieve crosstalk coupling of less than 1%

Channel Design

- **•General Channel Design Guidelines**
  - For high-speed transceiver signals, use trace widths of 6mils or more to minimize conductor loss.
  - Limit use of 4-mil trace widths to the BGA breakout area and keep their trace length as short as possible.
  - Loosely coupled traces are easier to route and maintain impedance control but take up more routing area.
  - Tightly coupled traces saves routing space but can be difficult to control impedance.
  - Use strip-line routing to avoid FEXT concerns.
  - C-via optimization techniques • Reduce the via capture pad size
  - Eliminate all non-functional pads (NFP)
  - Increase the via anti-pad size to 40 or 50 mils
  - Lvia optimization techniques:
  - Eliminate and / or reduce via stubs
  - Minimize via barrel length by routing near the strip-line traces near the top surface layer and applying back-drilling
  - Add ground return vias within 35 mils of each signal via to further improve the insertion and return losses of the via.
  - DC blocking capacitor compensation.

Sample checklist for PCB Layout

Signal and Power Integrity
Check whether test coupon/structure, if any, covers enough variety of the PCB, such as single-ended vs. differential, top layer vs. middle layer, etc.
High speed trace via stub lengths are less than 10 mils. Back drilling is used for vias with stub lengths higher than 10 mils.
Return loss is < -12dB for all high-speed diff. pairs
Planes used for power delivery of all rails. If a plane is not possible, sufficiently wide traces are used (width > 100 mils)
Capacitor pad is connected to power and ground plane with larger vias to minimize loop inductance
Wide - short traces are used between the vias and capacitor pads or vias are placed adjacent to capacitor pads
Power supply sense lines are connected very close to the load
High frequency decoupling capacitors are placed very close to device

Routing and Placement
There are no 90-degree corners on traces
High speed traces routed on impedance-controlled layers
Multiple vias on high-speed traces and clock lines are avoided
High speed differential pairs are not routed close to clock lines
GND vias are placed close to single ended and differential signal vias
Stitching vias are used to tie all GND planes.
Stitching via diameter roughly equal to trace width
Each GND pin or via are connected to plane individually
High speed traces are not routed near or across discontinuities in the reference plane such as splits or voids
High speed traces are not routed over an antipad

Sample checklist

Differential Pair Design
Skew between P and N signals of a differential pair are matched
Skew between P and N signals are matched on a per layer basis
Differential vias are placed as a pair in a symmetrical fashion
Spacing between differential pairs is 3X higher than spacing between P & N traces to reduce cross talk
P and N traces of a differential pair are routed on the same layer
Width and Spacing of the differential pair P and N traces are as per fab vendor specification
High current power rails are not routed close to TX or RX differential pairs
Impedance variation is less than +/- 10%

Signal and Power Integrity
Check whether test coupon/structure, if any, covers enough variety of the PCB, such as single-ended vs. differential, top layer vs. middle layer, etc.
High speed trace via stub lengths are less than 10 mils. Back drilling is used for vias with stub lengths higher than 10 mils.
Return loss is lower for all high-speed diff. pairs
Planes used for power delivery of all rails. If a plane is not possible, sufficiently wide traces are used (width > 100 mils)
Capacitor pad is connected to power and ground plane with larger vias to minimize loop inductance
Wide - short traces are used between the vias and capacitor pads or vias are placed adjacent to capacitor pads
Power supply sense lines are connected very close to the load
High frequency decoupling capacitors are placed very close to device

Sample checklist

Mechanical
Connectors/ switches/sockets have sufficient clearance space around them
Adequate number of mounting holes are present
If a socket is used, sufficient clearance space is provided around DUT
If a socket is used, socket mounting hole locations are verified to be correct
If SMA connectors are used, there is sufficient clearance space between SMAs for handling
A heatsink if required can be attached without any issues

Thank You

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