MoSys Accelerator Engine Overview

Topics

- **Introduction to Acceleration**
  - Memory Tradeoffs vs Performance
- **Accelerator Engines Integrated Circuits**
  - Quazar Family
  - Blazar Family
  - Accelerator Engine Architecture
    - Quad Partition Rate Memory
    - Intelligent In-Memory Function Bandwidth Accelerators
  - Application Examples using Accelerator Engines
- **Architecture Impacts Performance**
  - Tapping the power of FPGAs
  - On chip intelligence
- **Programmable HyperSpeed Engine (PHE) - Brief Introduction**
- **Stellar Packet Classification IP – Brief Introduction**
  - Scalable Deep Header / Deep Packet Inspection
  - Millions of Rules
  - 100's of Millions of Searches per Second
- **LineSpeed – 100G PHY ICs**
- **Applications and Use Cases**

Accelerator Engines & Linespeed Product Lines

QUAZAR FAMILY of Integrate Circuits

Memory

Performance/Cost Target Memories

Quad Partition Rate Engine (QPR)

QPR4 576Mb memory
QPR8 1Gb memory

Low Cost QDR alternative
- Replace 4 QDRs
- **For less than $200 in volume**

Higher bandwidth
- Up to 240Gb/s

Lower power

Pin compatible with BLAZAR family

BLAZAR FAMILY of Integrate Circuits

Accelerator Engines (AE)

Memories with Embedded Acceleration Engines

Bandwidth Engine (BE)

BE2 576Mb memory
BE3 1Gb memory

QPR **PLUS** Acceleration
In-Memory Acceleration Functions
Two options
- Burst (12+ functions)
- RMW with ALU (17+ functions)

Programmable HyperSpeed Engine (PHE)
- Same as BE3 (1Gb memory)
- **PLUS** 32 RISC CPU cores

LINESPEED Integrated Circuits

Networking Signal Management

Retimers, Gearboxes, Mux/Demux for Line Cards and Modules

Gearboxes

100G Gearbox
- with and without RS-FEC

100G Multi-Link Gearbox (MLG)
- 10 x 10GbE Breakout

Retimers

Protocol Independent Retimer
100G (4x25G) Retimer
- with and without RS-FEC

10-Lane Full Duplex 25G Retimer

Mux/Demux

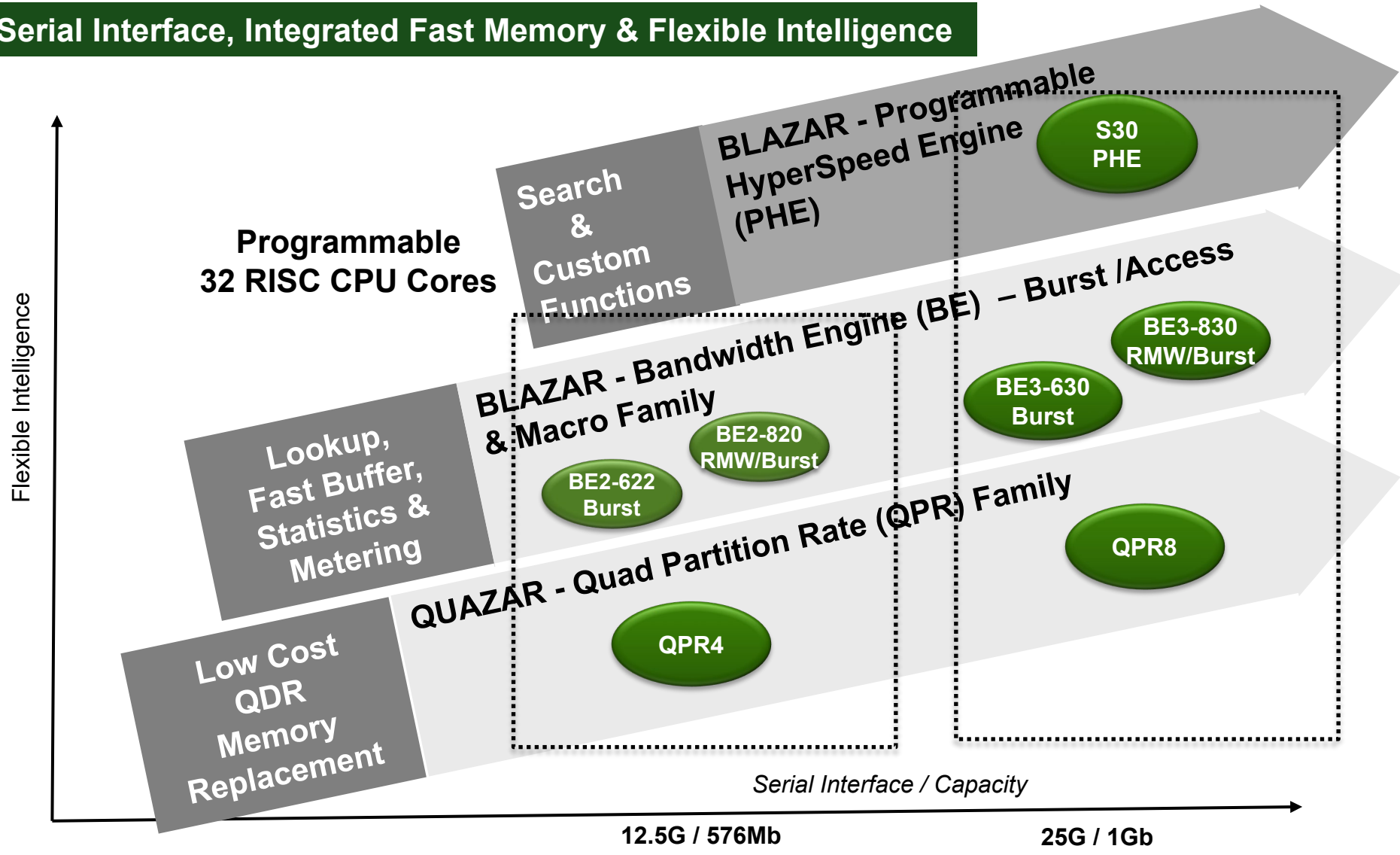
2:1 Serial Multiplexer/Demultiplexor
- Redundant Link Mode option

STELLAR FAMILY of FPGA/ASIC IP

Virtual Accelerator Engines (VAE) - ***IP that is Scalable and Portable***
Based on GME (Graph Memory Engine) **Packet Classification Platform**

QUAZAR and BLAZAR Families
Intelligent Offload

Serial Interface, Integrated Fast Memory & Flexible Intelligence



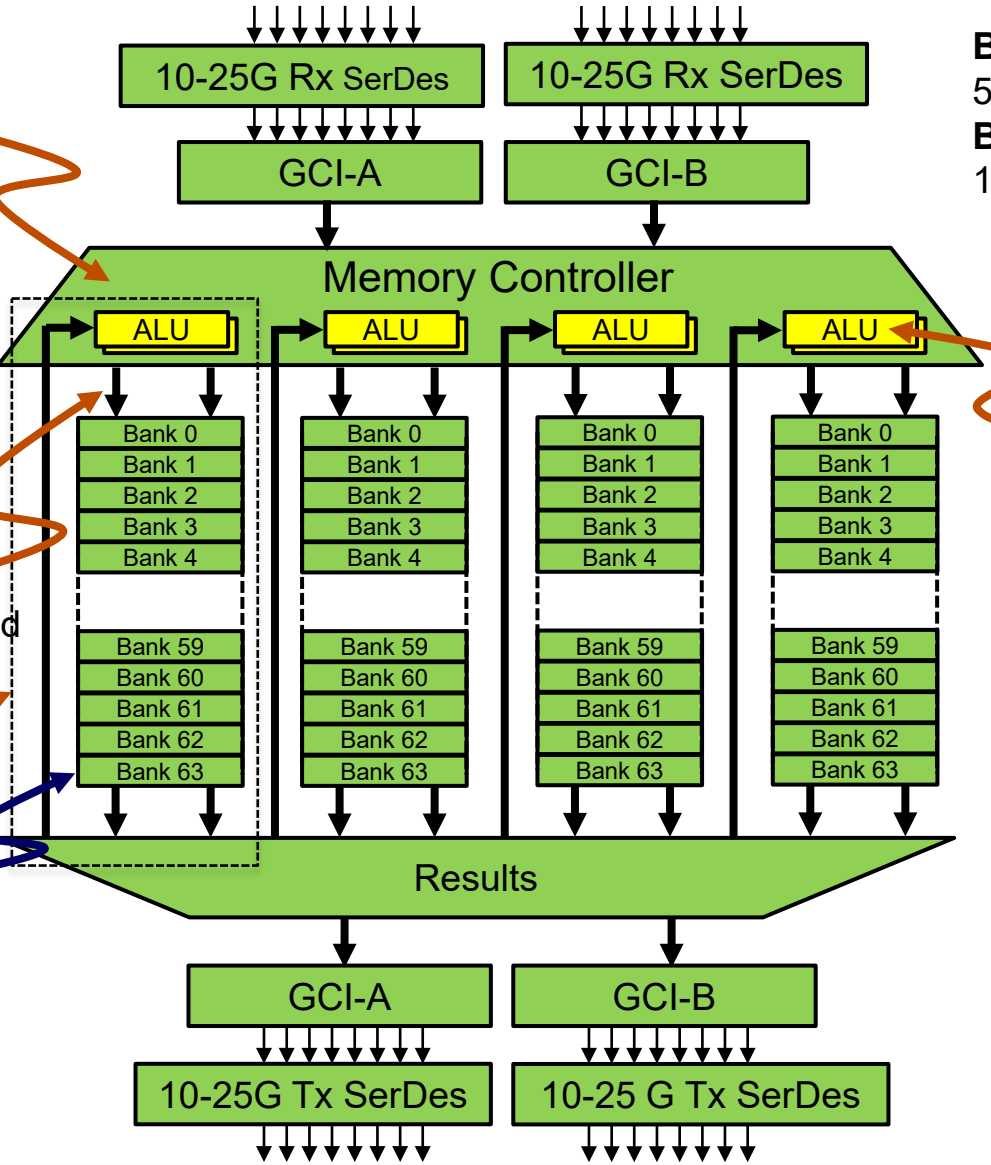
Memory Type – Architecture Achieving Performance and Bandwidth

UNDERSTANDING YOUR APPLICATION IS KEY!

Accelerator Engine Performance Based on Architecture

QPR4/8
Memory Ops:
Rd/Wr 72b
Wr 36b

BE2:
576Mb, 4 Partitions, 64 Banks
BE3:
1Gb, 4 Partitions, 128 Banks



BE2/3 BURST
In Memory Functions
8/16 Reads
8/16 Writes

BE3 - Double the Read & Write capability

Partition

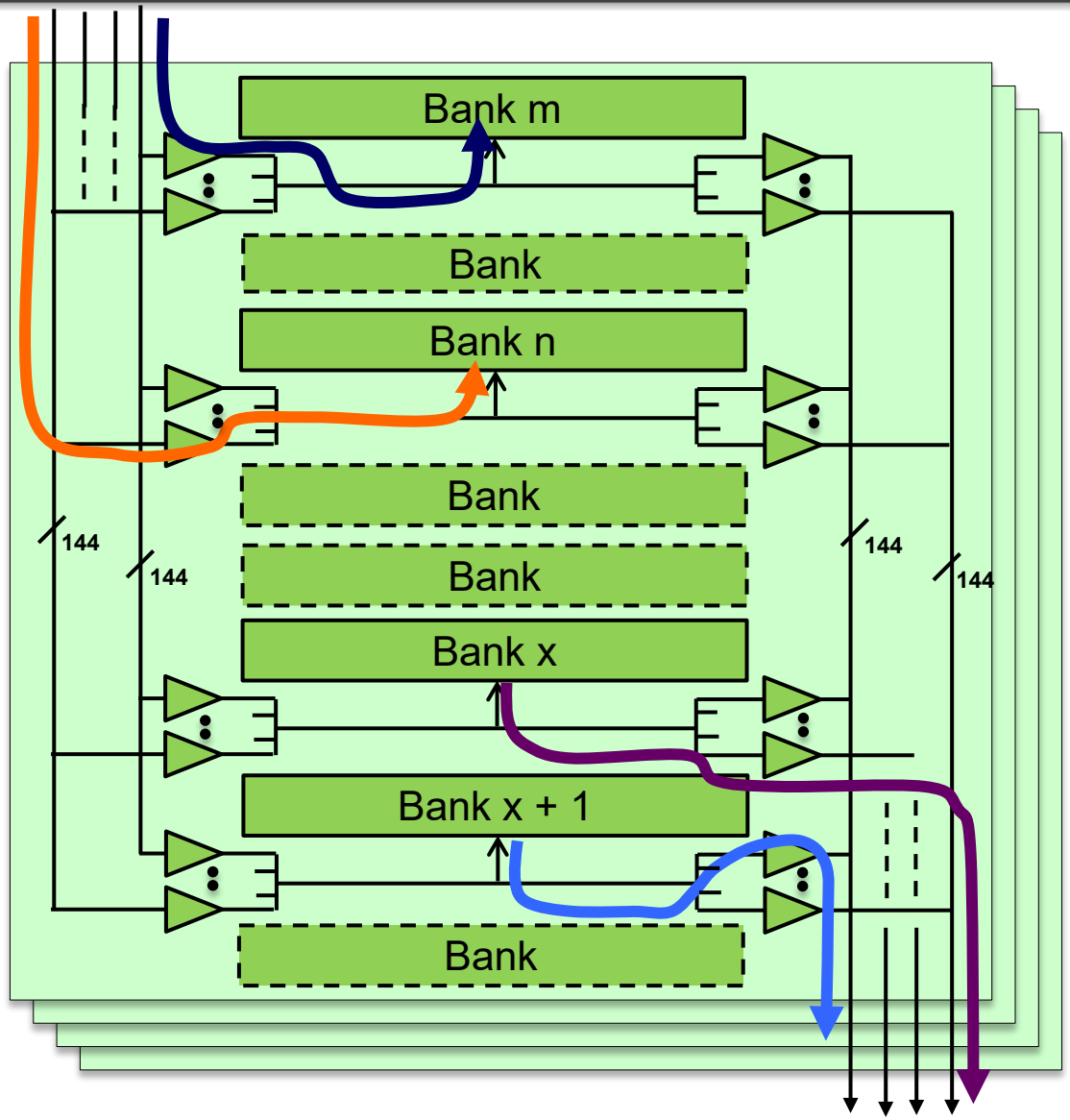
Banks

BE2/3 RMW
In Memory Functions
Incr/Decr
Dual Incr
Metering
Test & Set
Read & Set
More…

4 Partitions Achieve 6B Reads & 6B Writes per second ➔ >1.7 Tbps

4 ports @ 144b
X 4 Partitions

864 Gbps



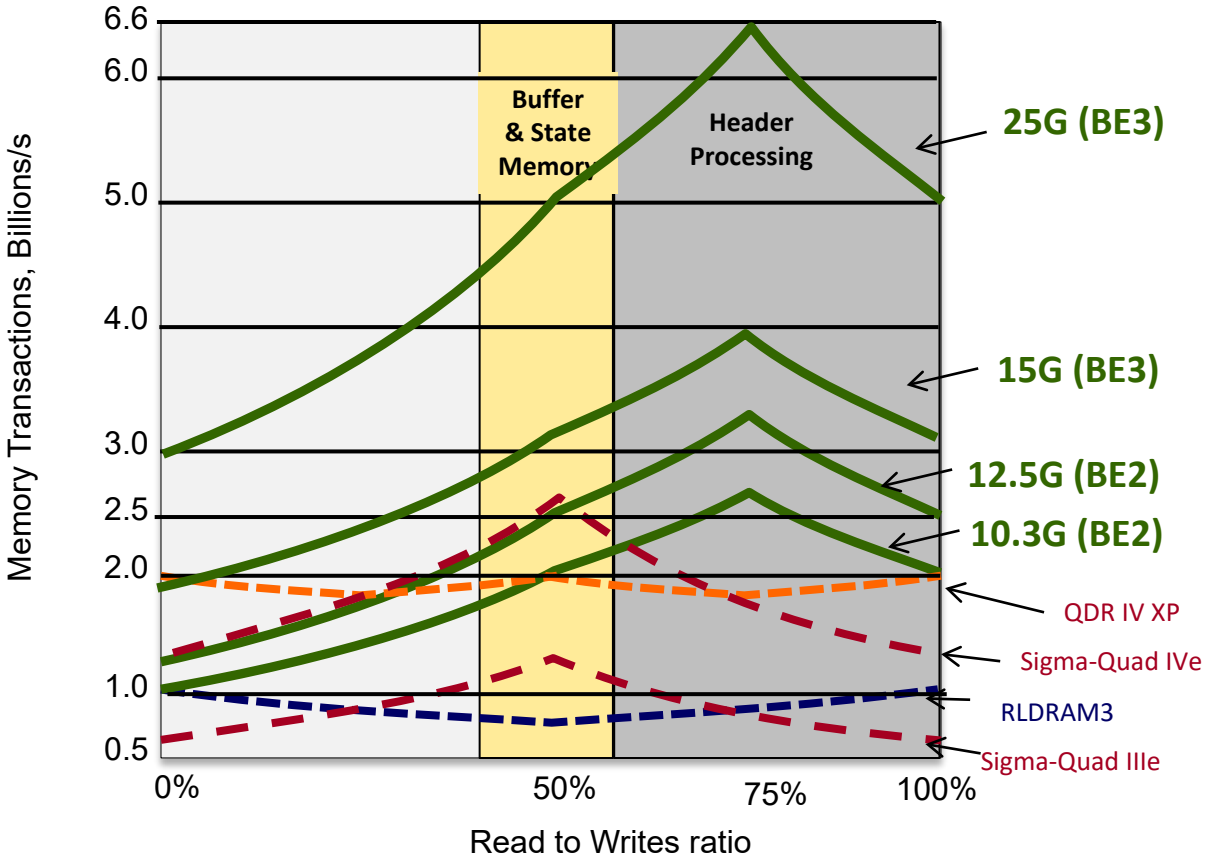
375MHz

4 ports @ 144b
X 4 Partitions

864 Gbps

BE2/BE3: 72b Access Performance

Application Dependent: High speed acquisition to packet inspection



MSR 622/820/630/830 Single Chip Buffering: Full Duplex Data Throughput

- **Effective throughput of payload; 72b per word**
  - BL# = Burst length; linear burst of 2, 4 or 8 words
- **Full duplex: balanced read and write**

Throughput (Gbps)		Speed Grade			
		622-10	622-12	630-15	630-25
Width	Burst	10.3125G	12.5G	15G	25G
16 lane	BL8	132.0	**160.0**	**192.0**	**320**
	BL4	118.8	144.0	172.8	288
	BL2	99.0	**120.0**	**144.0**	**240**
8 lane	BL8	66.0	**80.0**	**96.0**	**160**
	BL4	59.4	72.0	86.4	144
	BL2	49.5	60.0	72.0	120
4 lane	BL8	33.0	**40.0**	**48.0**	**80**
	BL4	29.7	36.0	43.2	72
	BL2	24.8	30.0	36.0	60

Sigma Quad IVe BL4 is:
93 Gbps Full Duplex
(192 Gbps I/O throughput)
8 x 16Mb single ported banks
~4.5W (device + I/O)

QDR IV XP is:
76.5 Gbps Full Duplex
(153 Gbps I/O throughput)
8 x 16Mb single ported banks
~7W (device + I/O)

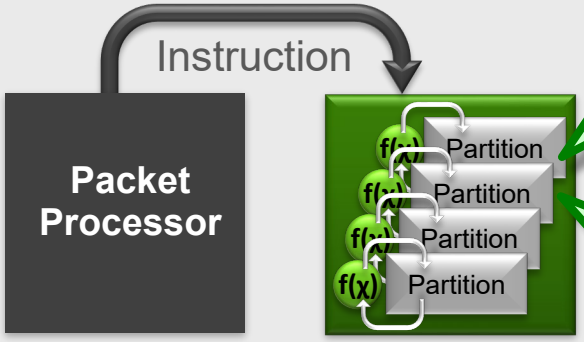
RLDRAM 3:
33 Gbps Full Duplex
(76.8 Gbps I/O throughput)
8 x 16Mb single ported banks
~3.5W (device + I/O)

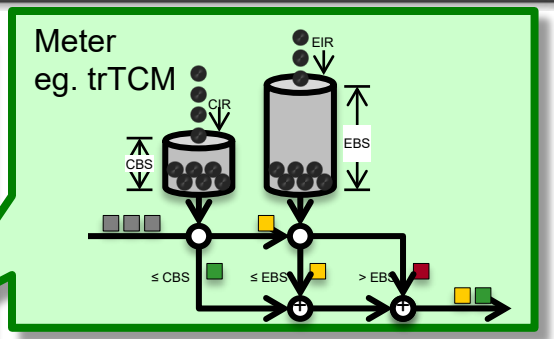
Typical Bandwidth Engine Applications

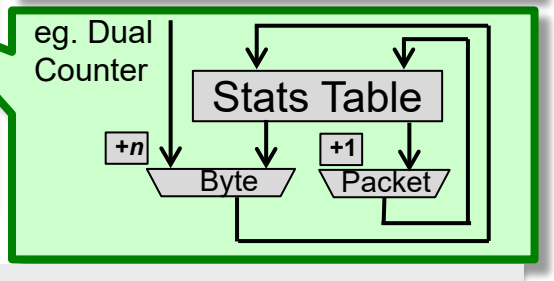
The Bandwidth Engine delivers the Highest Performance of any External Memory

- Most Efficient Interface Protocol
- Up To 25G IO Rates x 16 lanes
- Bandwidth of 640Gbps
- Sixteen concurrent memory ops
- Highest Look-Up Performance
  - ➢ up to 5 billion reads per second

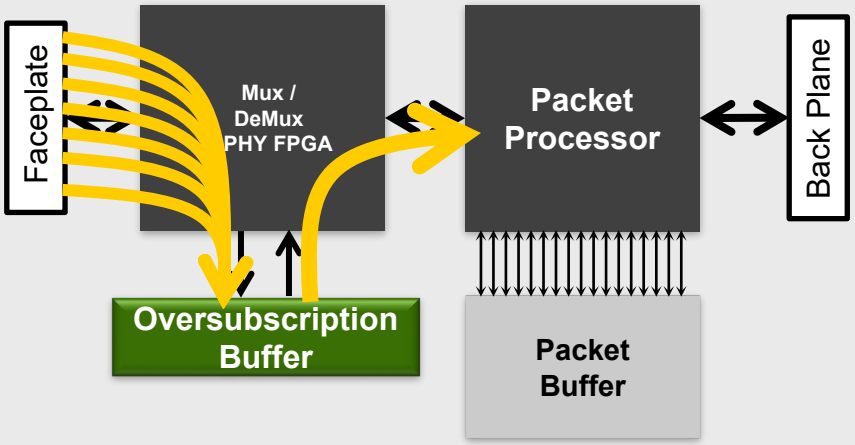
Intelligent Offload – 32 x 100G



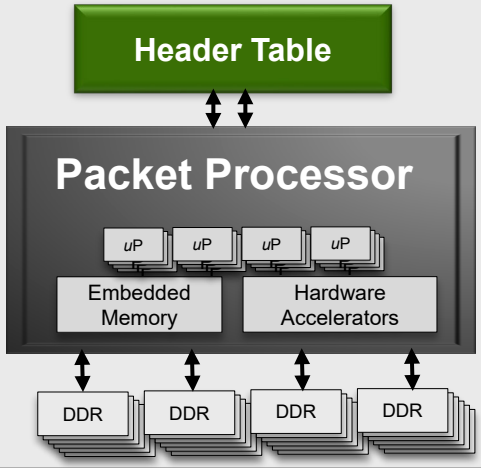




Single Chip - 400 Gbps FDX buffer

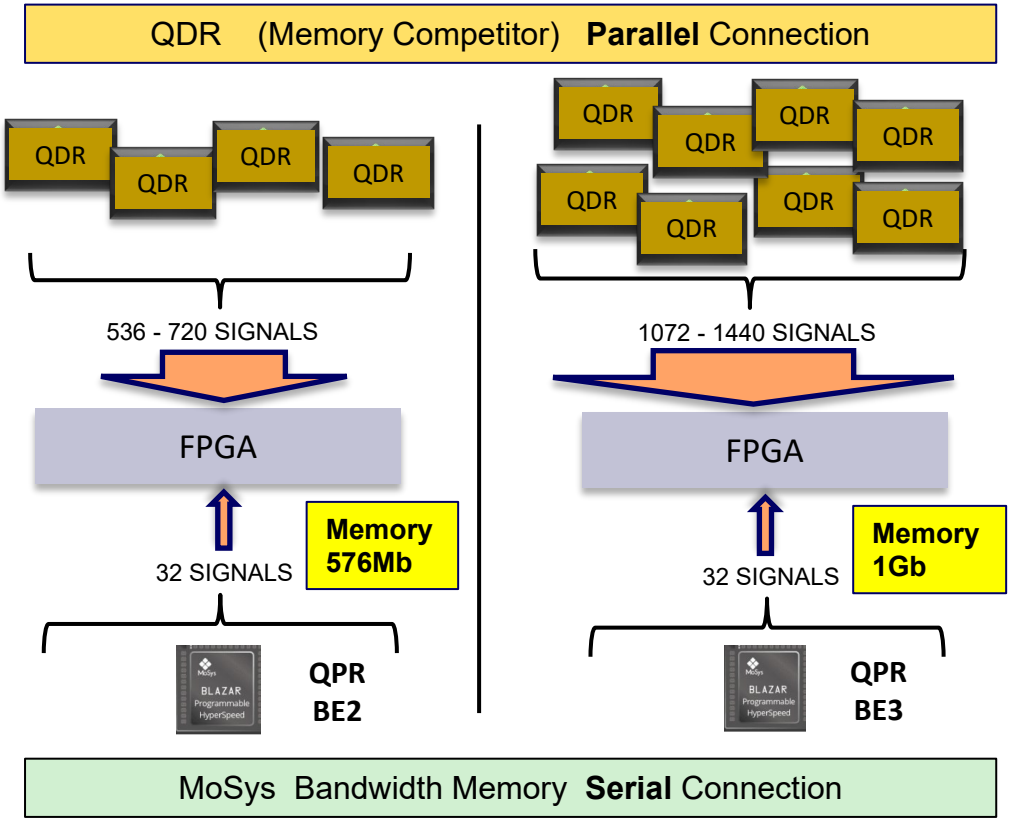


High Access Rate Tables– Up to 5B Reads/s



Memory Architecture is Critical
Increase Performance AND Save Space/Cost

Parallel vs Serial



Space & Cost Considerations

Performance Balance of Memory vs Space

- Space and Memory Capacity
  - One QPR/BE2 = 4 QDR … 512Mb
  - One QPR/BE3 = 8 QDR … 1Gb
- Part Cost
  - 1-QPR/BE2 for 576Mb memory ~ 2x cost of one QDR
    - 4x Memory
  - 1-QPR/BE3 for 1Gb memory ~ 2.5x cost of one QDR
    - 8x Memory
- Design time
  - Reduces signal routing time and layout
  - Told it saved 6-9 months
- Signal Integrity
  - Comparable QDR system has 536-1440 clean signals generally requiring external components
  - MoSys system typical has 32 signals with on board Auto-Adaptation signal tuning
    - No external components
- Power
  - ~ Half
- Bandwidth
  - Random data access is equivalent (tRC 2.7-3.2 ns)
  - For certain applications, much faster

1st Polling Question

- **Q1) Do you have high bandwidth FPGA applications (80Gbps or above aggregate line rates)?**
  - I design 80Gbps or above aggregate line rate boards for either Test & Measurement, Networking, Security
  - I am considering using TCAMs
  - My application includes Packet Header Inspection, Payload inspection, Look Up Tables
  - My application may need small (5-10ms) ingress or egress smoothing buffers

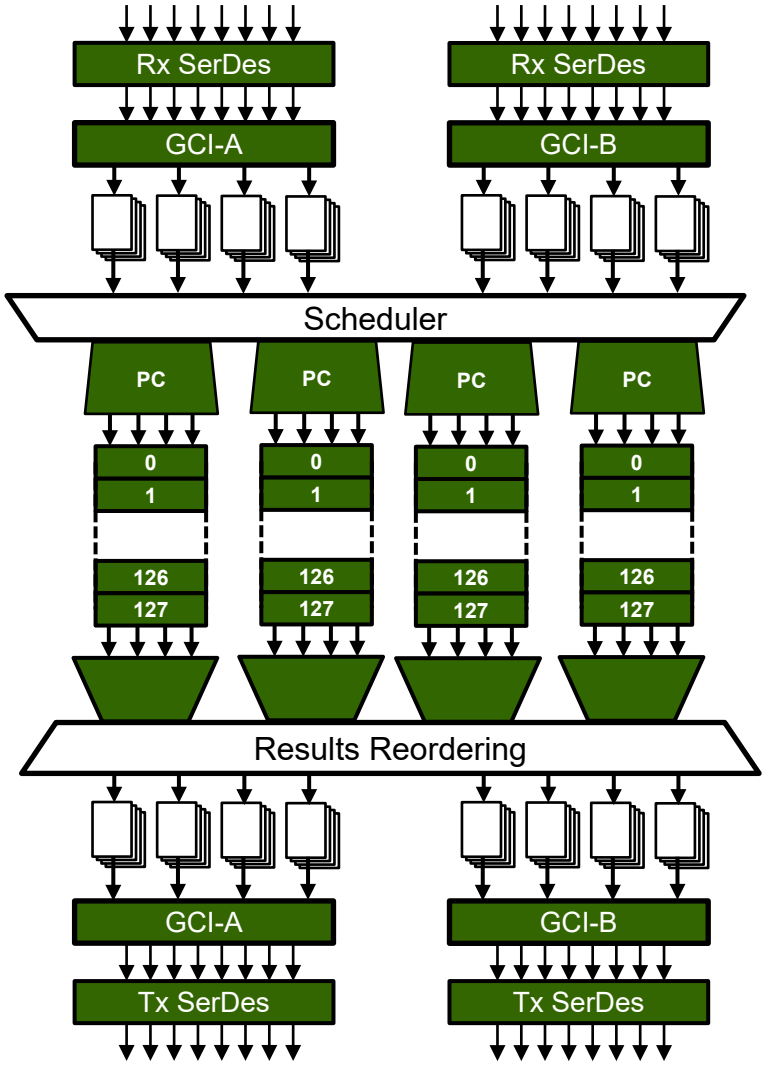
Performance impact of In-Memory Functions BURST-RMW

LET YOUR MEMORY DO THE WORK!

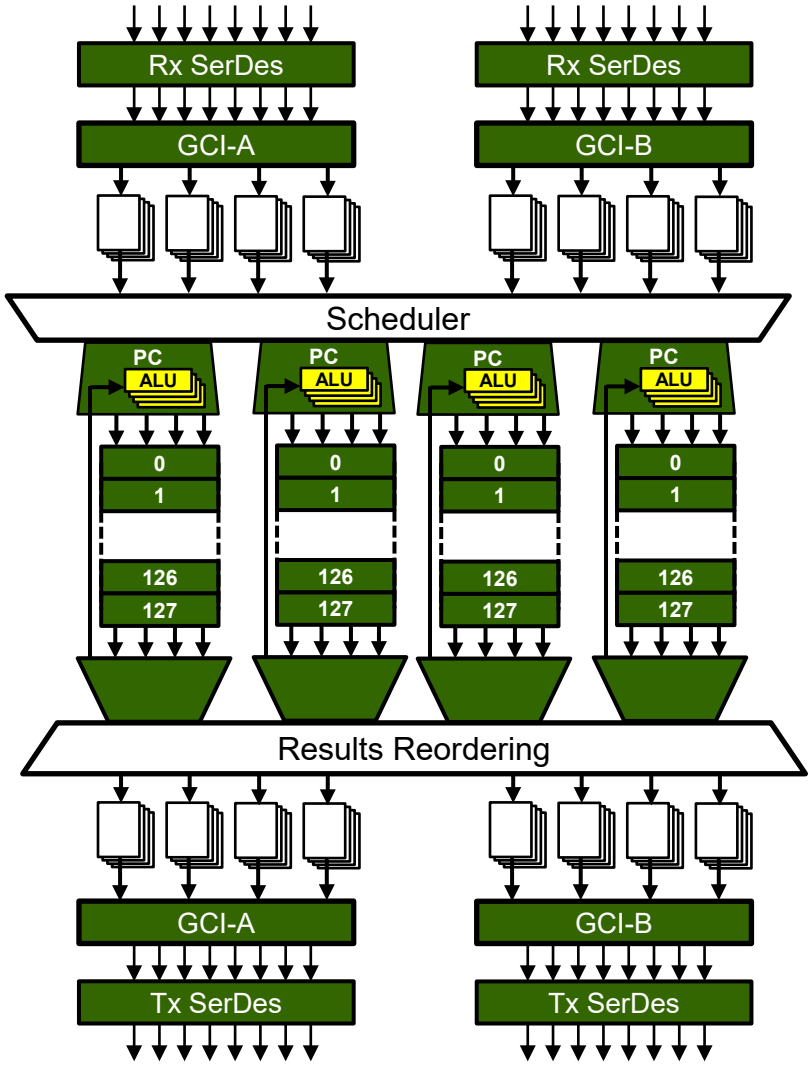
BE3 - BURST

MSR630 – Bandwidth Engine IC

- Fast, Efficient Serial Interface
  - 16 lanes, 12-15G, 20-25G SerDes
  - Independent GCI Ports
- Highest Performance Single Chip Transaction Rate Memory
  - 1Gbit memory capacity
  - 5+ billion transactions/sec
  - 32 ported memory array architecture
  - 3ns memory cycle time
- Burst Mode Capable
  - Burst of 2, 4, or 8
- Testing modes
  - PRBS generation and checking
  - Loopbacks
- Small form factor
  - 27x27mm package



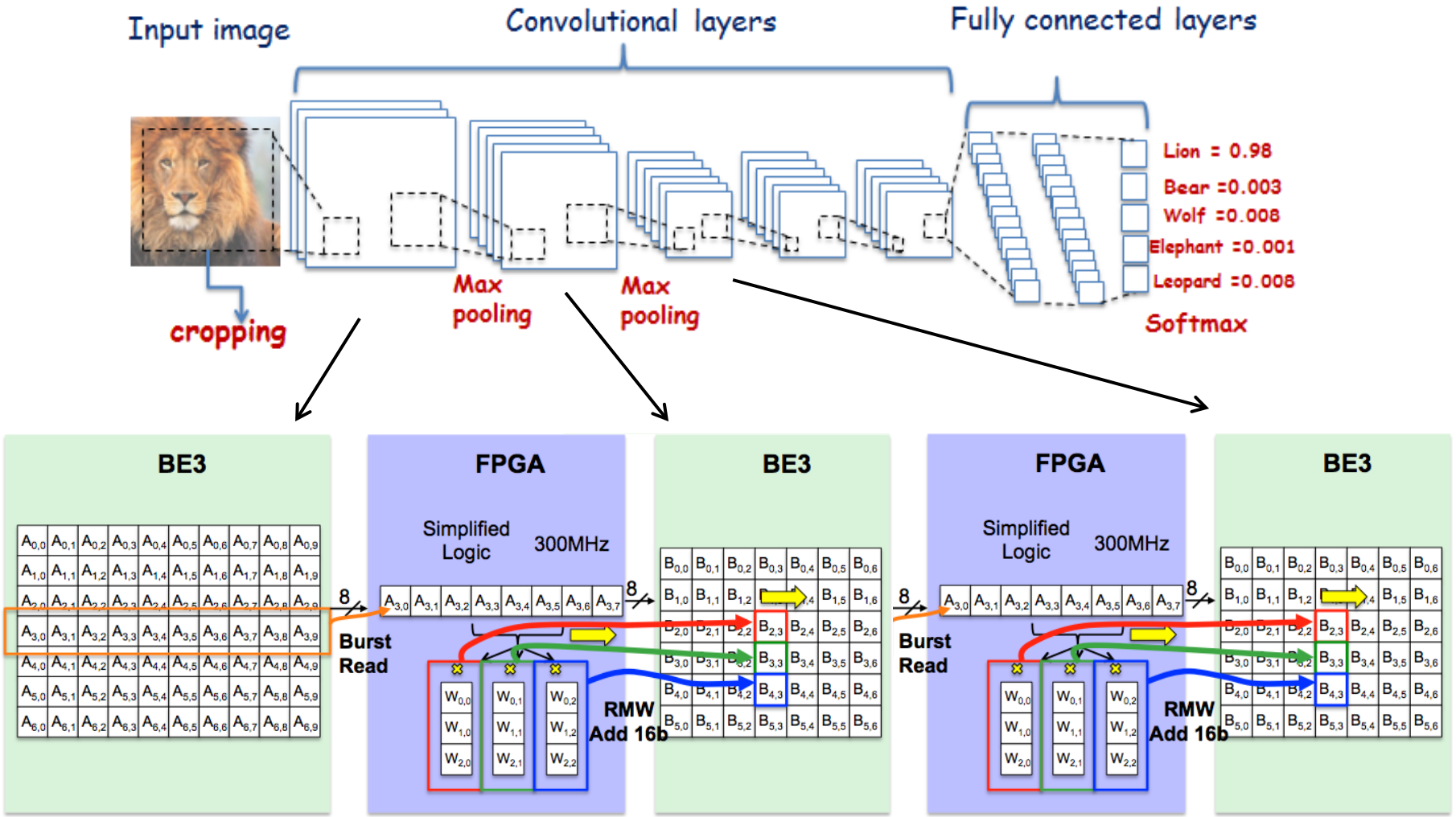
BE3 – RMW



BE with Intelligent Offload

- Fast, Efficient Serial Interface
  - 16 Lanes, 12-15 or 20-25Gb/s
  - Independent GCI Ports
- Intelligent Macro Offload
  - Multiple ALUs per Partition
  - Built in Memory coherent statistics, Metering and atomic operations
- Macro optimize transaction efficiency
  - Low pin count but high performance
- Highest Performance Single Chip Transaction Rate Memory
  - 1Gbit memory capacity
  - 5+ billion transactions/sec
  - 32 ported memory array architecture
  - 3ns memory cycle time
- Burst Mode Capable
- Small form factor
  - 27x27mm package

Pipelining With BE3 As A Dual Port



2nd polling Question

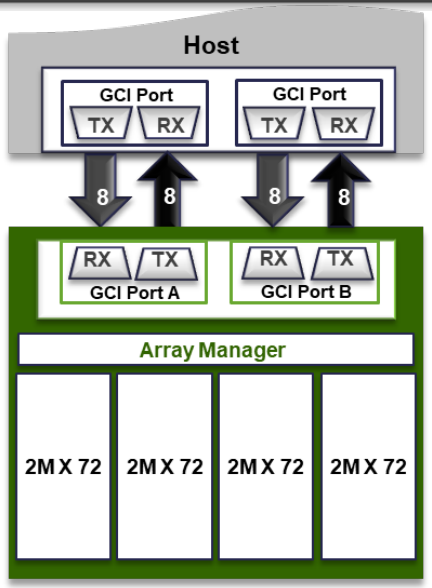
- Q2) Do you have a design that uses QDR or SyncSRAM that would benefit by having more High Speed Memory than the QDR provides?

  - I use 1 QDR and would benefit by having 2 to 4 x the density
  - I use QDR for the access speed but the density is limiting
  - I use multiple QDR devices but the routing is impacting my PCB design
  - QDR answers all my needs at this time

QUAZAR Family Architecture

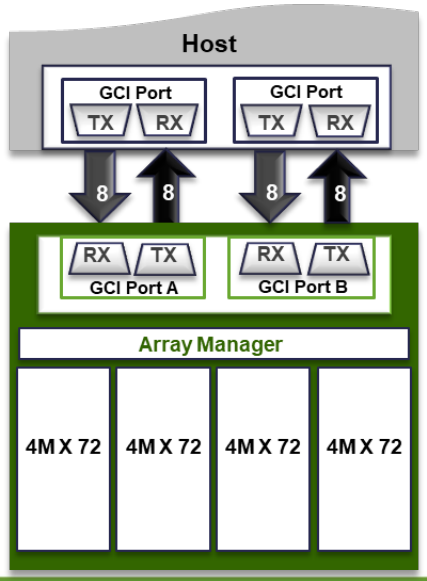
- **Low Cost QDR alternative**
  - Replace 4 QDRs for less than $200 in volume
- **Simple to use device**
  - 4 or 8 independent random-access SRAMs that can be accessed simultaneously in one cycle
- **576Mb and 1Gb capacity**
  - Single device
- **Low tRC (2.7 - 3.2ns)**
- **Higher bandwidth, Up to 640Gb/s**
- **Lower power**
- **Simplified design effort**
  - Two SerDes (GCI) Ports (Port A and Port B)
  - Up to 25Gbps SerDes
  - Memory Controller for Intel/Xilinx FPGAs provided

QPR4/8



- **Quad Partition Rate (QPR4)**
- **Parallel Array Architecture … Performance up to:**
  - 16 outstanding transactions
  - 2.5 Billion Transactions per Second
  - 120 Gbps full duplex throughput
  - 16 ns deterministic read latency
  - 3.2 ns Random cycle time (tRC)

Applications	MSQ220	MSQ230
Lookup, LPM, Hash	Highest single component Access Rate	
Small Table Structure	36 bit access	



- **Parallel Array Architecture … Performance up to:**
  - 32 outstanding transactions
  - 5 Billion Transactions per Second
  - 240 Gbps full duplex throughput
  - 16 ns deterministic read latency
  - 2.7 ns Random cycle time (tRC)

Applications	MSQ620	MSQ630
Lookup, LPM, Hash	Highest single component Access Rate	
Small Table Structure	36 bit access	

BLAZAR Family Architecture

- **576Mb and 1Gb memory devices**
  - Single device
  - Added features of Burst and In-Memory-Functions
    - Burst Up to 8 Words
    - ALU (R-M-W)
- **Simple QDR or SyncSRAM replacement**
- **Same simple FPGA to BE device interface**
  - Base use case uses only 32-pins to an FPGA
- **Low tRC of 2.7-3.2ns**
- **Bandwidth up to 640Gb/s**
- **Simplified design effort**
  - Two SerDes (GCI) Ports (Port A and Port B)
  - Up to 25Gbps SerDes
  - Memory Controller for Intel/Xilinx FPGAs provided

Benefits

- **System performance equal/better than a QDR**
- ***Costs significantly less than the equivalent density of QDR components***
- ***Greatly shortens design time***
- **Intel & Xilinx FPGA compatible**
- **In-Memory Acceleration Functions <u>Embedded:</u>**
  - All Bandwidth Engines (BE2, BE3, PHE)

    - BURST- single command Multi-word Read and Write
      - Buffering
      - High Speed Table Lookups

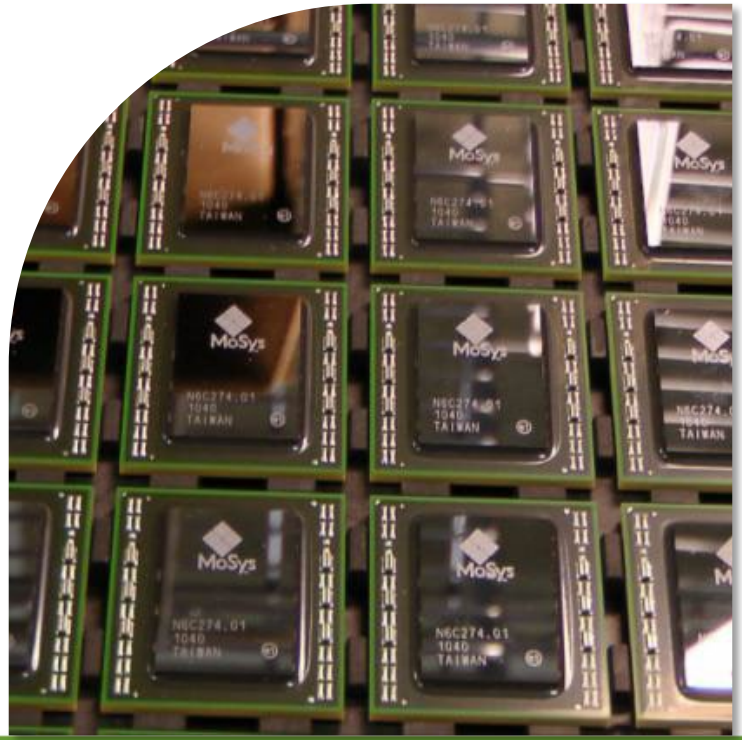
    - RMW – Single Read/Modify/Write commands
      - Statistics
      - Metering

Quad Partition Rate Family Status

- **QPR4**
  - 576Mb Memory
  - 4 QDR/SyncSRAM replacement
- **QPR8**
  - 1Gb Memory
  - 8 QDR/SyncSRAM replacement

- **QPR SerDes Interface**
  - MoSys GigaChip (SerDes) Interface support
    - Altera, Broadcom, eASIC, EZChip,
    - GSI, Macnica Americas, Xilinx

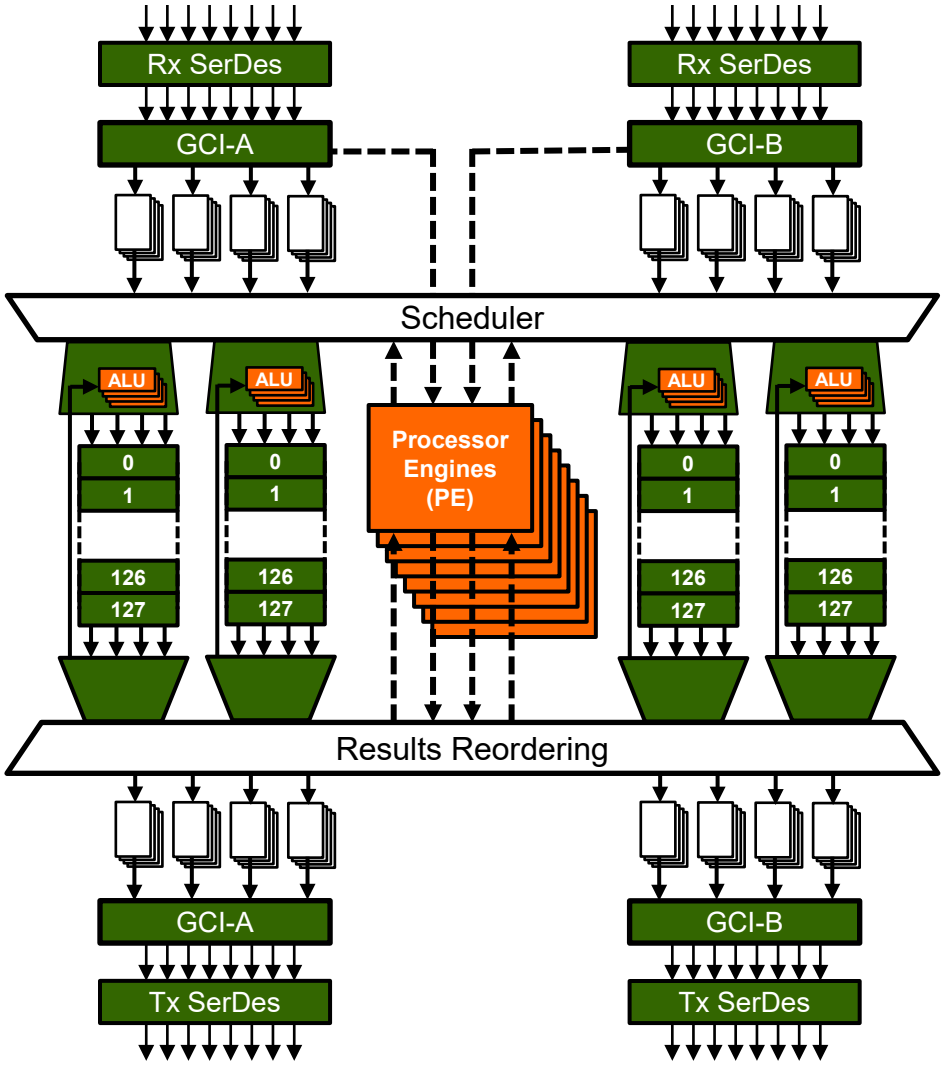
- **Qualified for Carrier & Enterprise Markets**
  - CRC and ECC end-to-end data integrity
  - Robust Error Immunity of 1T-SRAM
  - MoSys - ISO 9000 Certified
  - 100’s of thousands shipped, no returns



Programmable HyperSpeed Engine (PHE) Introduction

Programmable HyperSpeed Engine (PHE) Architecture

- **Physical**
  - 16 x 10 to 30Gbps PHY
  - SerDes Standard GigaChip Interface (GCI) Protocol
  - 8 Scheduling Domains
  - Integrated 1Gb Fast Memory
- **Threaded Processor Engines**
  - 32 cores (8 clusters of 4 PE)
  - Up to 1.5GHz
  - 8 threads per PE
  - Search-optimized ISA
- **Internal Performance**
  - 5B Rd/s + 5B Wr/s
  - 3ns tRC
  - Access up to 144 bits/cycle
- **676 FCBGA 27x27mm, 1mm**



Instruction Set Overview

- **ALU/Logical on 72b**
  - add, sub, adc, sbb, s1add, s2add, s3add, s3sub, and, or, xor, andn, sar, slr, sll, minu, maxu, mult
- **Bit field of variable len @ variable pos**
  - Extract, deposit, chomp
  - Can be across register boundaries
  - Optional auto incr of pos
- **Special Functions**
  - Find first zero, find first one
  - Population count
  - Swap bits in bytes and bytes in words
  - 144b HASH to 72b (non-crypto)
  - Compute CRC32
  - Mult-way compare with 4, 6, 9 & 12 inputs
- **Test & Branch**
  - tsteq, tstgt, tstnle, tstlt, tstnge, tstgtu, tstnleu, tstltu, tstngeu, tstbs, tstne, tstle, tstngt, tstge, tstnlt, tstleu, tstngtu, tstgeu, tstnltu, or tstbc
  - Jmp, jeq, jgt, jnle, jlt, jnge, jgtu, jnleu, jltu, jngeu, jbs, jne, jle, jngt, jge, jnlt, jleu, jngtu, jgeu, jnltu, or jbc
  - Multiway branch 2, 3 & 4
- **Loads & Stores**
  - Local Dmem:
    - 8, 16, 32, 64 & 72b
    - Reg + offset, w/auto incr reg
  - Partition:
    - Burst reads, load balanced reads and broadcast
    - 64, 72, 128, 135, 144b
    - Reg + reg or reg + offset, w/auto incr reg
- **Atomic Operations**
  - Local:
    - 8, 16, 32 & 64b
    - adda, suba, anda, xora, andna, xchga, cmpxchga
  - Partition:
    - 16, 32, & 64b
    - Add(s), sub(s), xor, rd/set, tst/set, cmp/set, avg, tm, age
- **Program Control**
  - Hlt, Brk & nop
  - Add/mov & halt (tread)
  - Yield
- **Special registers**
  - GPR indirect specification
  - Auto increment
  - Command, memory, result, result len
  - Time stamp, random, zero, all ones, thread id, wake up, sink

Accelerator Engine Devices

In-Memory	Part Number	Description	Package	Interface						Memory		Access Rate	In-Memory Functions		
			Pkg Size	Lanes	Rate per Lane Gb/s				BW MAX.	tRC	Size	Billion Transactions per second	R/W	BURST for Data Movement	RMW / ALU for Compute and Decision
			mm	Tx/Rx	10.3	12.5	15.6	25	Gb	ns	Gb				
QPR4	MSP220	QPR4 (Quad Partition Rate) 0.5 Gb	FCBGA 19X19	16	✓	✓			120	3.2	O.5	2.5	✓		
QPR8	MSP230	QPR8 (Quad Partition Rate) 1Gb	FCBGA 27X27	16			✓	✓	240	3.2	1	4	✓		
BURST	MSR622	Bandwidth Engine 2 Burst Serial 0.5Gb High Access Memory	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓	
	MSR630	Bandwidth Engine 3 Burst Serial 1Gb High Access Memory	FCBGA 27x27	16		✓	✓	✓	640	2.7	1	6.5	✓	✓	
RMW	MSR820	Bandwidth Engine 2 RMW Serial 0.5Gb High Access Memory with ALU for RMW functions	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓	✓
	MSR830	Bandwidth Engine 3 RMW Serial 1Gb High Access Memory with ALU for RMW functions	FCBGA 27x27	16		✓	✓	✓	640	2.7	1	6.5	✓	✓	✓
Program	MSPS30	Programmable HyperSpeed Engine Serial Interface, 1Gb Memory, 32 RISC Processor cores for custom algorithms, compute, functions	FCBGA 27x27	16		✓	✓	✓	717	2.7	1	24 Internal	✓	✓	✓
RTL	RTL-AE	RTL Memory Controller for Bandwidth Engine and QPR (Quad Partition Rate) Memories	FPGA RTL Code		✓	✓	✓	✓			576Mb & 1Gb	6.5	✓	✓	✓

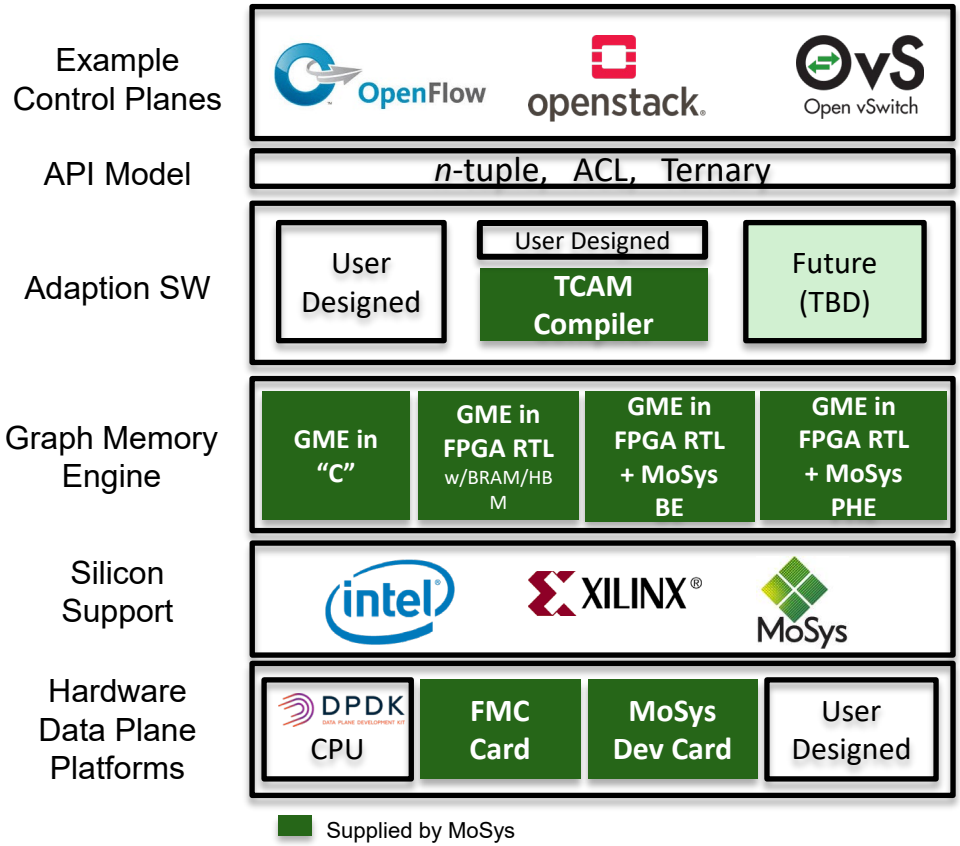
BW MAX. = Aggregate of all SerDes lane at the highest serial interface speed

3rd Polling Question

- **Q3) Do you need Packet Classification IP for your FPGA**
  - I would prefer to use FPGA RTL IP and on chip SRAM and/or external DRAM to do Packet Classification and Search vs. external TCAMs
  - I will implement Exact Match, LPM and/or ACLs
  - I need to use HBM already so Packet Classification IP that can leverage this would be valuable
  - I will implement Security functions like Firewalls, Anti-DDoS

STELLAR PACKET CLASSIFICATION PLATFORM IP for FPGAs

MoSys Packet Classification Platform



STELLAR - Packet Classification IP Platform

- **Supplied as FPGA RTL for Intel or Xilinx FPGAs**
- **Ultra High-Speed Search Engine IP**
- **TCAM-like functions**
  - Supports n-tuple ACLs & LPM search
- **Optimized to use High-Speed Memory**
  - Internal FPGA
  - Uses AND complements External memories (DDR, HBM, MoSys)
- **Graph Memory Engine**
  - Easy mapping of complex rules
- **Very fast updates**
  - Dynamically updated on the fly
- **Performance**
  - Up to multigigabit TCAM equivalence
  - Millions of rules
  - Hundreds of Millions searches per second

Two Editions: for LPM & ACL Applications

High Performance - LPM Edition

- Tuned for High Performance Routing Lookups using Longest Prefix Match (LPM)
  - Any mix of IPV4 and IPV6 lookups
  - Optimized for 1 or 2 tuple matches
  - Supports virtual routes

Applications:

- Cloud & Enterprise Datacenter Routing
- 5G User Plane Function (UPF) Routing
- Carrier-Grade NAT
- Broadband Network Gateway (BNG)
- Cloud Gateways
- Network Classification & Flow Steering
- L3 Forwarding & Filtering
- vRouter & Open vSwitch Offload
- Adding Routing to a SmartSwitch

High Flexibility / High Complexity – ACL & LPM Edition

- Tuned for Highly Complex n-Tuple Access Control Lists (ACL) rule lookups
  - Ideal for Security Applications
  - Optimized for complex 5 - 10+ tuple matches
  - Also supports Exact Match and routing lookups using Longest Prefix Match (LPM)

Applications:

- Network Security,
- Next Gen Firewall (NGFW)
- Anti-DDoS, Allow/Deny Lists
- Lawful Intercept
- L4 Load Balancing
- Application Delivery Controllers (ADC)
- Traffic Analysis
- Applications and Network Analysis
- Telemetry, Test and Measurement

LineSpeed™ 100G PHY IC Family

Flexible Line Card & Module Solutions

LineSpeed™ 100G PHY ICs

Applications

- Extending Reach of High-Speed Serial Links
  - Retimers with up to 20 lanes at 28Gb/s
- QSFP28-based Optical Interfaces
  - 100G (4x25G) Retimer w/ and w/o RS-FEC
  - 100G Gearbox w/ and w/o RS-FEC
- Bringing High-Speed Links to low-cost FPGAs
  - Mux/Demux of low-speed I/Os into high-speed I/Os
- Breakout of 100G ports to 10 x 10Gb Ethernet
  - Multi-Link Gearbox (MLG), including SyncE support
- High-Availability Systems with Redundant Links

Key Features

- Family of Retimer, Gearbox, & Mux/Demux ICs
- Compliant to IEEE, ITU, and OIF standards
- 100G RS-FEC encoder/decoder (optional)
- Redundant Link Mode for Protection Switching
- Independent baud rates per lane
- Strong, self-adapting receive equalizers
- Built-in PRBS generation and checking
- Multiple packages for line cards and modules
- *Priced at less than $50 in volume*

Product Description					Functions								Reach	Supported Rates	
	Part Number	Description	TX/RX Lanes	Package	Gearbox	MLG	Retimer	10x10G Retimer	4x25G Retimer	Clause 91 RSFEC	Mux/ Demux	Redundant Link Mode	15-20dB w/o FEC	10-14G	25-28G
Retimers	MSH221SF	100G Octal Retimer w/ FEC	8	12x12mm			✓		✓	✓			✓	✓	✓
	MSH222S	100G Full Duplex Retimer	8	13x13mm			✓		✓				✓	✓	✓
	MSH222SF	100G Full Duplex Retimer w/ FEC	8	13x13mm			✓		✓	✓			✓	✓	✓
	MSH225S	10 Lane Full Duplex Retimer	20	17x17mm			✓	✓					✓	✓	✓
Gearbox	MSH320S	100G Gearbox	20	17x17mm	✓			✓					✓	✓	✓
	MSH320SF	100G Gearbox w/ FEC	20	17x17mm	✓			✓		✓			✓	✓	✓
	MSH321S	100G MLG Gearbox	14	12x12mm	✓	✓			✓				✓	✓	✓
	MSH322S	100G MLG Gearbox	14	17x17mm	✓	✓			✓				✓	✓	✓
Mux	MSH420S	10:5 Mux/Demux	20	17x17mm							✓	✓	✓	✓	✓
	MSH422S	4:2 Mux/Demux	8	13x13mm							✓	✓	✓	✓	✓

4th Polling Question

- Q4) ***Do you have any applications that may use 100G PHY retimer or gearbox devices?***
  - *I may use Gearbox – 4x25G to 10x10G Interfaces for 100GbE (with FEC option)*
  - *I may use Multi-Link Gearbox – 4x25G (Host) to 10x10GbE (SFP+ and/or QSFP+)*
  - *I may use a Retimer – 4x25G, 10x25G – full duplex, with 100Gb FEC option*
  - *I may need serial link redundancy and/or 2:1 multiplexing/demultiplexing*
  - *I use Broadcom, InPhi, Marvell 100G PHY devices and would consider an alternate source*

Bandwidth Performance Applications

Common Applications

- **Over-Subscription Buffers**
- **Maintaining Statistics**
  - Building Data Histograms
- **Fast Table Lookup Memory**
  - Routing
  - Switching
- **Load Balancing**
- **Image Processing**
- **Firewall - Security**
- **VAE (IP)**
  - TCAM replacement
    - ACL
    - LPM
  - DPI
- **Etc.**

Accelerator Engine Devices

In-Memory	Part Number	Description	Package	Interface						Memory		Access Rate	In-Memory Functions		
			Pkg Size	Lanes	Rate per Lane Gb/s				BW MAX.	tRC	Size	Billion Transactions per second	R/W	BURST for Data Movement	RMW / ALU for Compute and Decision
			mm	Tx/Rx	10.3	12.5	15.6	25	Gb	ns	Gb				
QPR4	MSP220	QPR4 (Quad Partition Rate) 0.5 Gb	FCBGA 19X19	16	✓	✓			120	3.2	O.5	2.5	✓		
QPR8	MSP230	QPR8 (Quad Partition Rate) 1Gb	FCBGA 27X27	16			✓	✓	240	3.2	1	4	✓		
BURST	MSR622	Bandwidth Engine 2 Burst Serial 0.5Gb High Access Memory	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓	
	MSR630	Bandwidth Engine 3 Burst Serial 1Gb High Access Memory	FCBGA 27x27	16		✓	✓	✓	640	2.7	1	6.5	✓	✓	
RMW	MSR820	Bandwidth Engine 2 RMW Serial 0.5Gb High Access Memory with ALU for RMW functions	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓	✓
	MSR830	Bandwidth Engine 3 RMW Serial 1Gb High Access Memory with ALU for RMW functions	FCBGA 27x27	16		✓	✓	✓	640	2.7	1	6.5	✓	✓	✓
Program	MSPS30	Programmable HyperSpeed Engine Serial Interface, 1Gb Memory, 32 RISC Processor cores for custom algorithms, compute, functions	FCBGA 27x27	16		✓	✓	✓	717	2.7	1	24 Internal	✓	✓	✓
RTL	RTL-AE	RTL Memory Controller for Bandwidth Engine and QPR (Quad Partition Rate) Memories	FPGA RTL Code		✓	✓	✓	✓			576Mb & 1Gb	6.5	✓	✓	✓

BW MAX. = Aggregate of all SerDes lane at the highest serial interface speed

Thank You