MoSys Newsletter
Accelerating Data Intelligence
www.mosys.com
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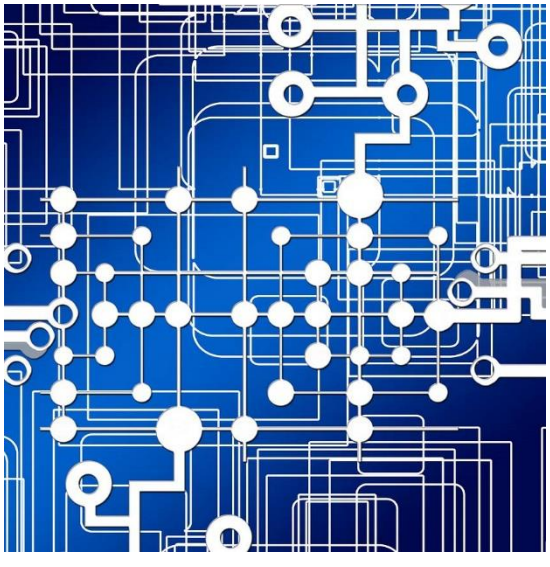
A Message from MoSys
News From Our CEO

Welcome to another edition of the MoSys newsletter. In this edition we are focusing on board design and best practices. With the chip shortage in full swing, extending your design is more important than ever and MoSys has a lot of best practices for board design that will help you economically extend your board design including:

- How to economically extend your design
- How board design can expediate your next design
- Best practices for board design
- High Speed board design guidelines and more

We hope you find this newsletter informative. Please feel free to provide feedback on the content or any new ideas that you might have.

Dan Lewis
CEO, MoSys, Inc.



News Alerts!

MoSys Silicon Chosen by APS Networks to Help Telcos Boost Number of Subscribers for Broadband Network Gateways
June 29, 2021

MoSys Announces Optimized P4 Pipeline Support for Stellar Packet Classification Platform IP for FPGAs
May 17, 2021

MoSys Expands Patent Portfolio with Purchase of Custom Algorithm Search Patents
April 12, 2021

MoSys Announces New, Low Price Point for Its LineSpeed™ Flex 100G PHY IC Product Family
Feb. 23, 2021

MoSys and Arrow Electronics Collaborate to Optimize System Memory on FPGA Designs
Jan. 11, 2021

Multiplexing and Demultiplexing High-Speed Serial Links with MoSys LineSpeed™ Flex PHY
Oct. 22, 2020

100G Gearbox with RS-FEC Solution for QSFP28-Based Optics with the MoSys LineSpeed™ Flex PHY IC
Sept. 30, 2020

MoSys Design Support Center

Board Design Made Easy

Best Practices for High-Speed Board Design

MoSys provides Printed Board layout recommendations for use with the MoSys® LineSpeed™, Bandwidth Engine® (BE), and Programmable HyperSpeed Engine (PHE) high-speed serial products.

Both signal integrity and power integrity guidelines are provided. The emphasis is on the signal integrity, as it is generally easier to achieve a decent power distribution on the board with multiple planes available and room for capacitors on both top and bottom. Read more: Download Board Guidelines

How to Expedite Your Next Design

In our webinar, which can be viewed on the Arrow.com website, topics commonly used in PCB designs that use SerDes were discussed such as:

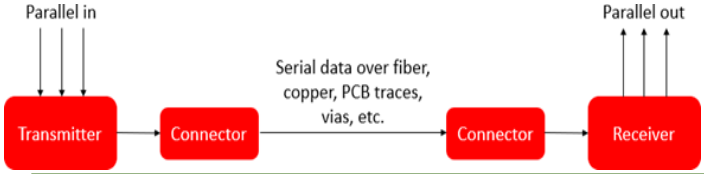
Insertion Loss which represents the loss of signal power resulting from the insertion of a device in a transmission line. Insertion loss is the ratio of the output signal to the input signal and it is measured in decibels (dB).

Return Loss which is a measure in relative terms of the power of the signal reflected by a discontinuity in a transmission line. The cause of this discontinuity can be any mismatch between the load connected to the line and the characteristic impedance of the line.

S-Parameters, or S (scattering) parameters can be used to characterize electrical networks. In this case, scattering refers to the way traveling currents or voltages are affected when they meet a discontinuity in a transmission line.

Crosstalk which refers to the unwanted transfer of signals between communication channels.

Read more: LINK



Focus on Use Case: Test & Measurement

In this case study, we will be looking at a test and measurement system that is used to develop statistics on a system with multiple ports of up to 100G Ethernet. The key challenge is to develop an FPGA-based card which can analyze and capture Ethernet data for line speeds of 10G,40G or 100G.

Key Points Summary:

- Highest capacity single chip high speed SRAM device available on the market (1.1Gb)
- tRC = 2.7ns
- Interfaces to the Host with CEI compliant SerDes
- Uses only 64 pins
- Can be accessed from two separate Hosts (Dual Ported)
- Low latency SerDes protocol allows for SRAM equivalent performance
- Proven to work with Intel and Xilinx devices
- Less than 50K LUTs to implement the memory controller and GCI serial protocol logic
- Pin compatible devices that enable Burst and ALU functions allow for system feature enhancements without PCB redesigns
- Upgrade path for even higher performance: MoSys offers its Programmable HyperSpeed Engine (PHE) device in the same package as the BE3. The PHE has 32 embedded 8-way threaded 1.5Ghz core clock RISC engines to enable algorithm acceleration and 2x higher transaction rate for future proofing the design. Read more: LINK

Additional Resources:

Why is QDR is No Longer the Answer
One Device Using 32 I/O Pins that Replaces 4 to 8 QDR Devices
Memory Controllers Part 1 of 2
Memory Controllers Part 2 of 2
MoSys Bandwidth Engine vs. QDR

Email us and we will arrange to have one of our technical specialists speak with you. You can also sign up for updates. Finally, please follow us on social media so we can keep in touch.