Expanding High-Speed FPGA Memory

Use Case

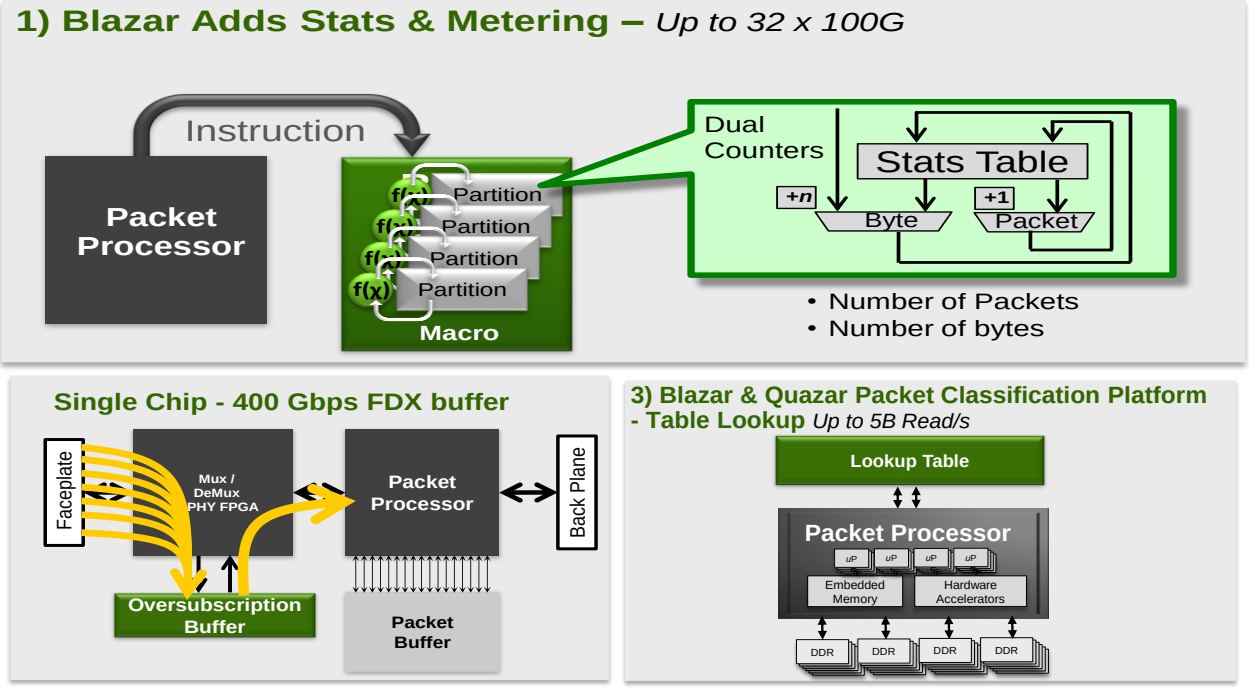
KEY CHALLENGES:

With the ever-increasing speed at which networks are running and the need for instantaneous access to data, it seems that there can never be enough memory. In most FPGA devices, the amount of high-speed SRAM like memory is now in the 300 to 400Mb range. This is rarely adequate for buffering, tables, statistics, etc. The predominant approach by the FPGA vendors has been to attach significant resources of High Bandwidth (HBM). Although this addresses some memory issues very well, it struggles to support high-speed, random access requirements.

To date, the approach has been to use QDR SRAM which provides high-speed memory access to an FPGA through a bus that is 100+ pins wide. Many customers are hitting limitations with the use of QDR. They need more high-speed, random access memory and the QDR is too shallow, uses too many pins, and is difficult to expand.

MoSys customers have substantially expanded their on-chip FPGA SRAM by replacing a single or multiple QDR devices with a single MoSys QPR (Quad Partition Rate) device or by adding MoSys QPR devices onto boards that had no high-speed external memory. The MoSys QPR devices offer 2 to 4x the on-chip FPGA memory density and 4-8x the attached QDR external memory capacity in a single chip. In both scenarios, using a MoSys device with a serial interface, saved them design time (both at the PCB level and the FPGA – RTL level), board space, routing complexity, general purpose IOs and in some cases, also reduced PCB layer count (reducing cost).

The unique interface of the MoSys Device (Giga Chip Interface - GCI) also allows for easy depth expansion of the external memory resource. By utilizing the same 16 SerDes lanes, the interface has allowed customers the ability to offer different performance and throughput SKUs of a single PCB by loading different numbers of MoSys devices on a card.



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KEY SYSTEM CONSIDERATIONS:

- Ease of design for use on network accelerator cards that are being deployed in many of today's 5G, Security, and edge routing systems
- The new FPGAs are increasing the number of SerDes lanes available over HSTL interfaces
- It is common for algorithms to need millions of rules and the ability for extremely fast rule updates
- Typical applications like Exact Match, ACL, Firewall and DDoS require millions of rules and high-speed random access to tables
- Typical multi-100Gbps network accelerator cards quickly overrun the available memory on an FPGA
- Designers need a proven, reliable way to expand the available High-Speed, random access memory available on an FPGA
- Interfaces to MoSys Memories can be implemented with as few as 20K ALMs or LUTS:
  - A single Monolithic MoSys device is equivalent in density to 4 or 8 QDR type devices
  - By utilizing SerDes as the interface I/O standard, designers can save design time, board routing space, power, and time to market
  - Using a MoSys memory enables functional upgrades by utilizing In-Memory-Functions available on MoSys pin-compatible devices
  - Provides a simple, single chip complement to on-chip FPGA memory

MOSYS SOLUTION

The MoSys Bandwidth Engine (BE) and QPR family of products provides High Flexibility/High Density devices that complement the on-chip memory found on an FPGA. It offers a proven, highly reliable high-speed, low latency random access expansion of the available FPGA memory. As many as 6.5B accesses a second can be achieved on a single device. The unique use of SerDes is a natural fit for the FPGAs with high SerDes counts.

High Flexibility/High Density Memory Devices

- Ultra-High-Speed Random Access
- High Reliability with Low SER
- Single monolithic 576Mb or 1.1Gb devices
- tRC as low as 2.6ns
- Light weight, Low Latency Interface protocol (GCI)
- All devices are shipping in production
- Pin compatible devices allow for system feature upgrades
- FPGA – RTL change is all that is needed to upgrade from a straight High Speed Memory to an intelligent High Speed Memory with built in functionality of Burst, ALU's or embedded RISC cores
- Designs support replacement of QDR devices
- Some very popular applications:
  - Oversubscription Buffers
  - High Speed Table Lookups
  - FPGA Memory Expansion
- A secondary benefit of having two GCI Ports is the ability to use the device as a Dual Port
- Provides scalable performance when coupled with MoSys' Stellar Family of Packet Classification FPGA IP
  - Uses Graph Memory Engine (GME)
  - 100s of Millions of lookups per second
  - Millions of Rules
  - Low latency solution
  - Very efficient memory usage
  - Extremely efficient use of logic gates

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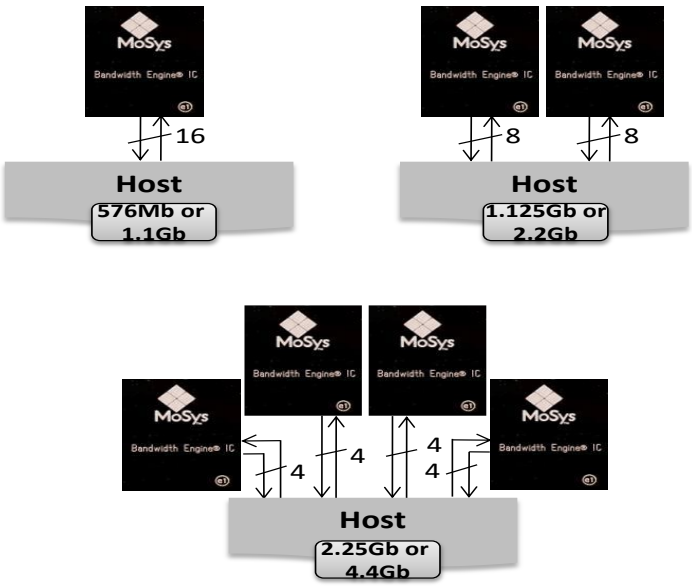
KEY POINTS SUMMARY:

- Very High-Access Rate Memory solution designed to complement and expand the memory resources that are available on an FPGA
- Very flexible design – MoSys Memory Controller IP easily integrated with either sample or custom controller code options available
- Takes advantage of available SerDes I/O resources in an FPGA or ASIC
- Helps future proof designs by supporting standard Read-Write memory access and allowing the ability to up grade to in-memory-functions like burst, ALU (R-M-W) and even an upgrade to a 1.1Gb capacity device with 32 RISC cores to run custom algorithms via MoSys pin-compatible devices.



ADDITIONAL RESOURCES:

Why Use SerDes to Talk to Memories? – Part 1 of 2

Why Use SerDes to Talk to Memories? Part 2 of 2

Why 8 Transceivers Per Port?

One Device Using 32 I/O Pins that Replaces 4 to 8 QDR Devices

MoSys New Quazar Solutions: 4 to 8 times as Many QDR SRAMs in a Single Package

Memory Controllers Part 1 of 2 & Memory Controllers Part 2 of 2

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