Test & Measurement Use Case
MoSys Bandwidth Engine + FPGA

Use Case

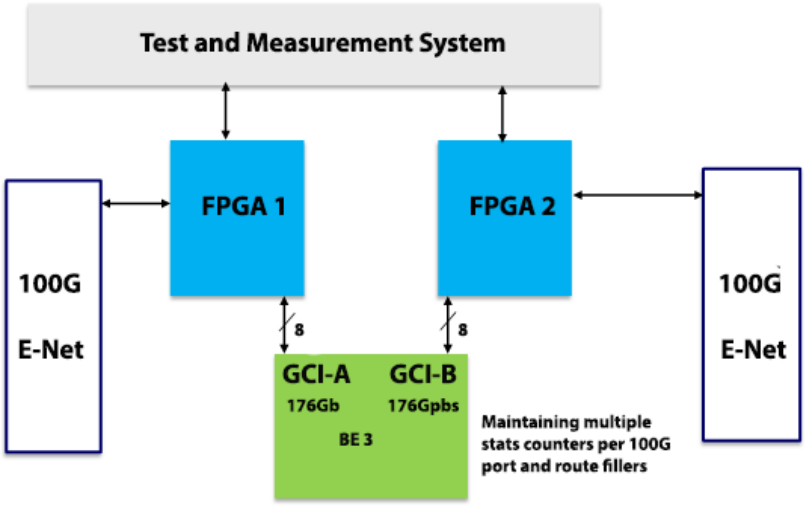
KEY CHALLENGES:

In this case study, we will be looking at a test and measurement system that is used to develop statistics on a system that interfaces with multiple ports of up to 100G Ethernet. The key challenge is to develop an FPGA-based card which can analyze and capture Ethernet data for line speeds (10G\40G\100G).

The Ethernet data shall be monitored based on filtering criteria. The filtering can be based on any number of criteria such as VLAN, IP, Port number, etc., or using a combination of any of these. Once the filtering criteria is matched, the system will then analyze the traffic and take the required data analytics.

The required throughput data dedicated a capture of up to 576 bits per packet and a read of up to 576 bits per frame. This requirement is per GCI Port of the Bandwidth Engine or the equivalent of 176Gb per port on the BE3 device, (352 Gb per BE3 device).

The BE3 device offers the ability to support counter adjustments when utilizing the on chip ALU function. In this case, the device is used to store the counter data that is adjusted by the host.



MOSYS SOLUTION

Because of the amount of logic needed to perform the other packet manipulation functions and because of the number of high speed SerDes needed for Ethernet and memory interfaces, the desired FPGA is an UltraScale+ or Stratix 10 class device.

This proposed solution allows the customer to successfully build a subsystem card that achieves the desired bandwidth to support multiple 100Gb interfaces and utilizes a significantly lower number of FPGA I/O resources and LUTs to build the required memory controller.

The Block Diagram in the figure above shows how the two 100G Ethernet ports are linked through the FPGAs to the two ports of the MoSys Bandwidth Engine. The Dual-Ported capability of the Bandwidth Engine 3 was also helpful in requiring only one device to handle multiple ports.

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	Requirement	Approach / Comment
1	An FPGA which has the bandwidth to support multiple Ethernet data for line speeds (10G\40G\100G)	Intel® Stratix 10® & Xilinx® UltraScale™ + families have the appropriate amount of logic and high speed SerDes lanes
2	Must maintain line speed	Use one GCI Port per 100G Ethernet port to support up to 176 Gb of data
3	Interfaces with the high-speed Transceivers on Stratix 10 and UltraScale + class FPGAs	The BE3 device is CEI compliant up to 25Gbps (NRZ)
4	Provide independent memory access from two sources	The BE3 device is capable of supporting access to the memory array from two independent hosts (even if running at different SerDes Rates)

KEY POINTS SUMMARY:

- Largest single chip high speed SRAM device on the market (1.1Gb)
- tRC = 3.2ns
- Interfaces to the Host using CEO compliant SerDes
- Uses only 64 pins
- Can be accessed from two separate Hosts (Dual Ported)
- Low latency SerDes protocol allows for SRAM equivalent performance interface
- Proven to work with Intel Stratix 10 and Xilinx UltraScale+ class devices
- Less than 50K LUTs to implement the memory controller and GCI serial protocol logic
- Upgrade path for even higher performance: MoSys offers its Programmable HyperSpeed Engine (PHE) device in the same package as the BE3. The PHE has 32 embedded 8 way threaded 1.5Ghz core clock RISC engines to enable algorithm acceleration and 2x higher transaction rate for future proofing the design

ADDITIONAL RESOURCES:

Stellar Virtual Acceleration Engines
Virtual Acceleration: The MoSys Approach
Cheetah Development Kit
High Speed PCB Design Guidelines
Why-use-serdes-to-talk-to-memories-part-1-of-2/
Why-use-serdes-to-talk-to-memories-part-2-of-2/
One-device-using-32-i-o-pins-that-replaces-4-to-8-qdr-devices/

2309 Bering Drive, San Jose, CA 95131
Tel: 408-418-7500
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