Packet Classification in 5G UPF (User Plane Function) Fixing LPM Routing Bottlenecks in New 5G Networks

Use Case

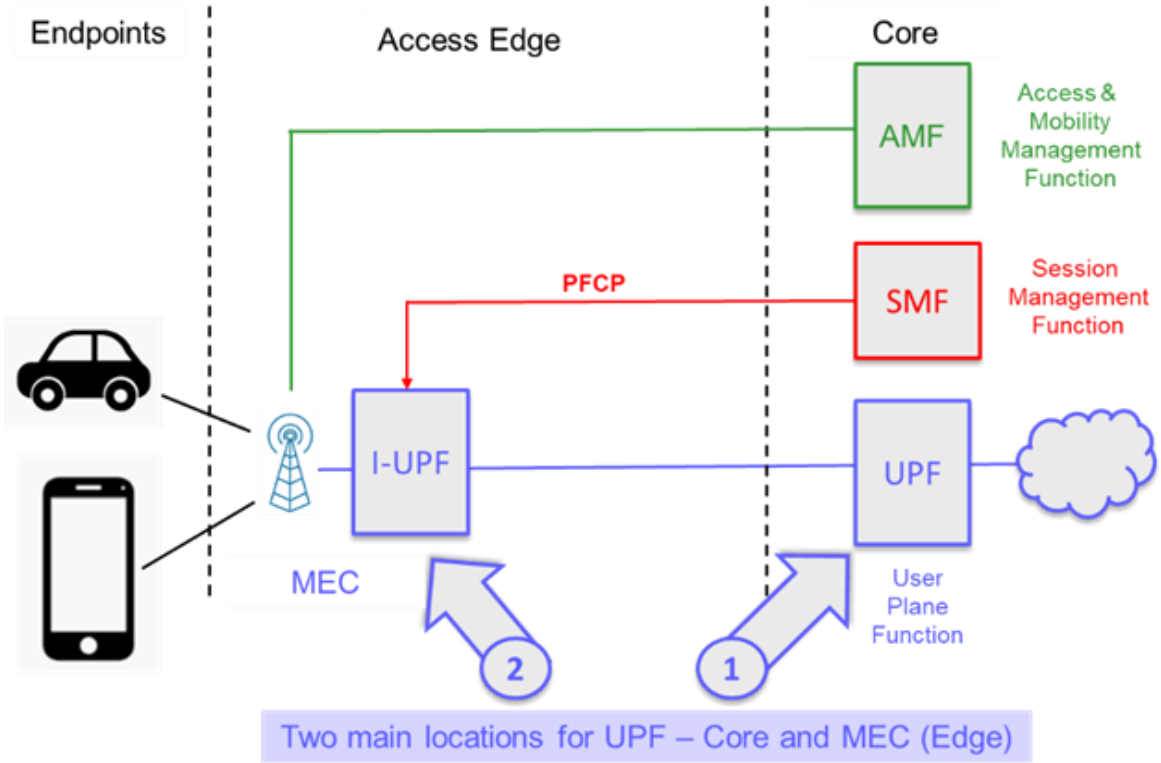
KEY CHALLENGES:

Data movement through the 5G network must meet certain time domain response requirements and one of the key bottlenecks is when data passes from the over the air portion to the wired network.

To meet these stringent requirements, it is key to understand how packet movement is done. The 5G User Plane Function (UPF) is the function that does all of the work to connect the actual data coming over the Radio Area Network (RAN) to the Internet. Being able to quickly and accurately route packets to the correct destination on the internet is key to improving efficiency and user satisfaction.

Routing requires that the headers of each packet are examined in real-time, this is called Deep Header Inspection (DHI) – and searches can use a combination of Exact Match, Longest Prefix Match (LPM) or even Access Control List match (ACL).

Depending upon the system, the total number of rules, the number of rules that match, the complexity of the rules and the speed of the searches (Millions of searches per sec) determine the overall performance level.



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KEY SYSTEM CONSIDERATIONS:

- UPF appears in 2 places – in the Core Network and at the Edge inside a MEC (Multi-Access Edge Controller)
- Deep Packet Header Inspection requirements - UPF can require millions of rules, none of which it learns, all of which come from Session Management Function (SMF)
- Typical 2 – 4+ Million rules – mix of IPV4 and IPV6 – same at Core and Edge
- Typical 50 – 400+ Million searches per second – higher perf at Core
- Typical 100Gbps to Terabits/s with low latency a must

Meeting the search requirements can be accomplished in several ways

- Execution in Software – but this can be too slow
- Using a standalone TCAM chip – but this can be high cost and high power
- Using a hardware accelerated Algorithmic TCAM in ASIC or FPGA
- Combining a multi-terabit SmartSwitch with any of the above

MOSYS SOLUTION

The MoSys Stellar Packet Classification Platform Intellectual Property (IP) uses a hardware accelerated Algorithmic TCAM-like approach to help ensure that the 5G UPF can keep up with the huge volume of routing decisions per second that it has to process.

High Performance LPM

- Ultra-High-Speed Search Engine IP
- Deep Header Inspection (DHI) solution
- Available for ASIC or FPGA
- Optimized for high performance routing
  - Can add other functions
  - Security, load balancing…
- Tuned for Longest Prefix Match (LPM)
  - Any mix of IPV4 and IPV6 lookups
  - Optimized for 1 or 2 tuple matches
  - Supports virtual routes
- Provides scalable performance
  - Uses Graph Memory Engine (GME)
  - 100s of Million lookups per second
  - Low latency solution
  - Very efficient memory usage
  - Extremely efficient use of logic gates
  - Very fast rule updates
  - No need to recompile rules
  - No need to preconfigure table sizes
  - On the fly updates – no need to stop traffic
  - Ability to receive updates from AI/ML logic
  - Supports large number of bits for next hop data
  - Capacities and key sizes beyond normal routing
- Supports broad range of devices
  - Can utilize hybrid mix of memories
  - Internal SRAM and/or external DDR, HBM
  - Can also use MoSys memories, but can operate without any MoSys silicon present
  - Supports RTL for Intel Stratix 10, Xilinx UltraScale+ FPGAs, or ASIC/SoC/DPU…
  - Replaces multiple expensive and power hungry TCAM chips
  - Common API for software interface – easier to port applications
- Applicable to designs based on NIC, SmartNIC, DPU, Standalone SoC, SmartSwitch…

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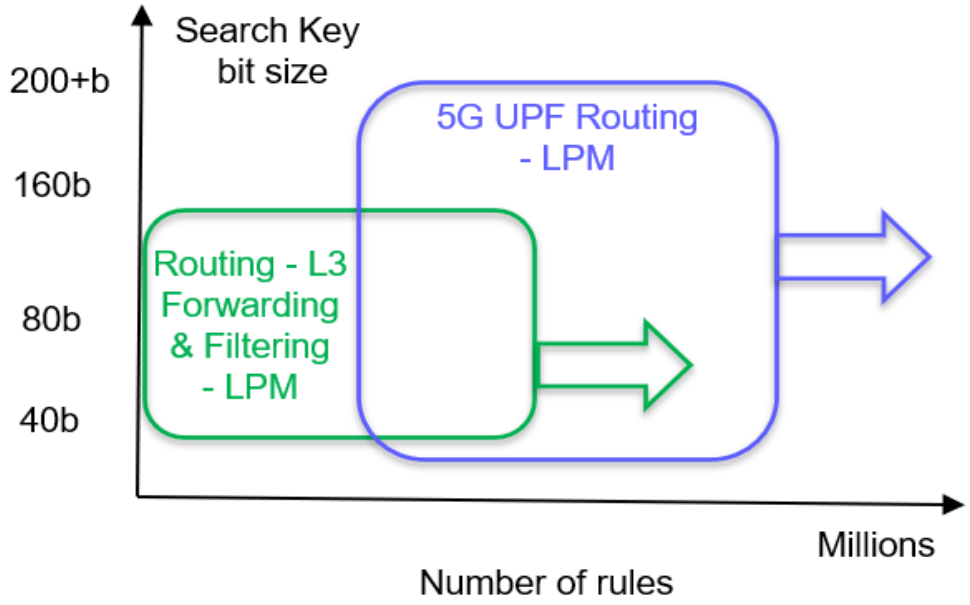
KEY POINTS SUMMARY:

- Very High-Performance solution designed to accelerate one of the main 5G bottlenecks – the 5G User Plane Function (UPF) – supports both IPV4 and IPV6 routes
- Very flexible design – MoSys IP easily integrated
- Takes advantage of available gates and memory in FPGA or ASIC
- Helps future proof designs by supporting wide range of key sizes, n+ tuple looks ups, very large number of rules at a very high performance in very efficient logic



ADDITIONAL RESOURCES:

Stellar Virtual Acceleration Engines
Stellar Virtual Acceleration Platform
Virtual Acceleration: The MoSys Approach
Cheetah Development Kit

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