MSH420 – LineSpeed™ Serial Multiplexer / Demultiplexer

PRODUCT BRIEF

MSH420 DEVICE OVERVIEW

The MoSys® LineSpeed MSH420 device supports the multiplexing and demultiplexing of two lower-speed serial links onto a single link at twice the baud rate. As physical interfaces on switching and packet processing ICs move to 25G PHY interfaces for performance and board density, the mux/demux function allows lower-speed and lower-cost FPGAs to support such high-speed interfaces.

MSH420 DESCRIPTION

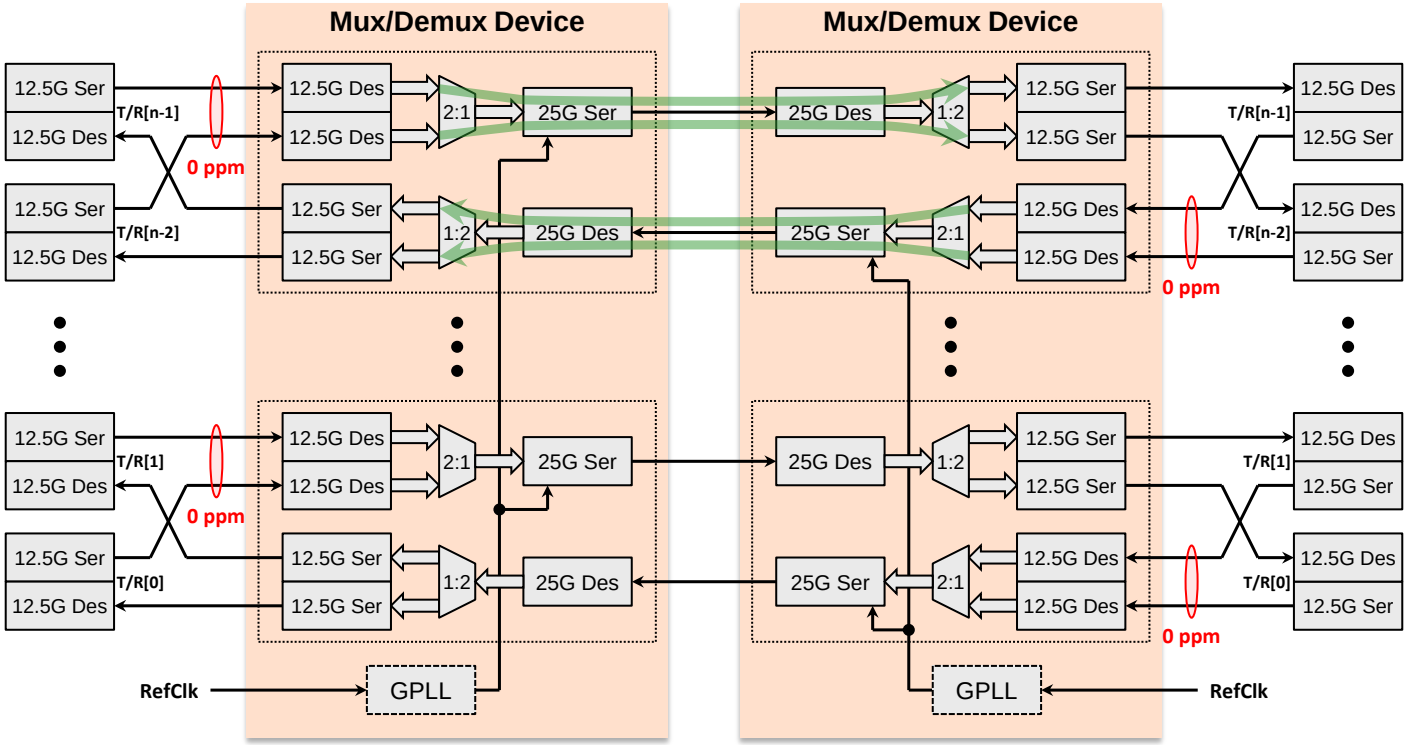
The MSH420 has a “bit-level” 2:1 serial Mux/Demux function which is agnostic to the data payload of the two lower-speed links. However, they must be operating at the same baud rate (i.e. “0 ppm” frequency offset). The MSH420 includes optional Retimer and Redundant Link modes (contact factory). The electrical interfaces support IEEE and OIF-CEI-3.0 10/11G and 25/28G specifications.

Configuration of the device is supported through an I2C, MDIO or SPI interface and can be configured through a uC or external EEPROM.

The device supports extensive test and monitor functions including PRBS Generators and checkers, error and eye quality monitors, alarms, and MLG link monitor registers.

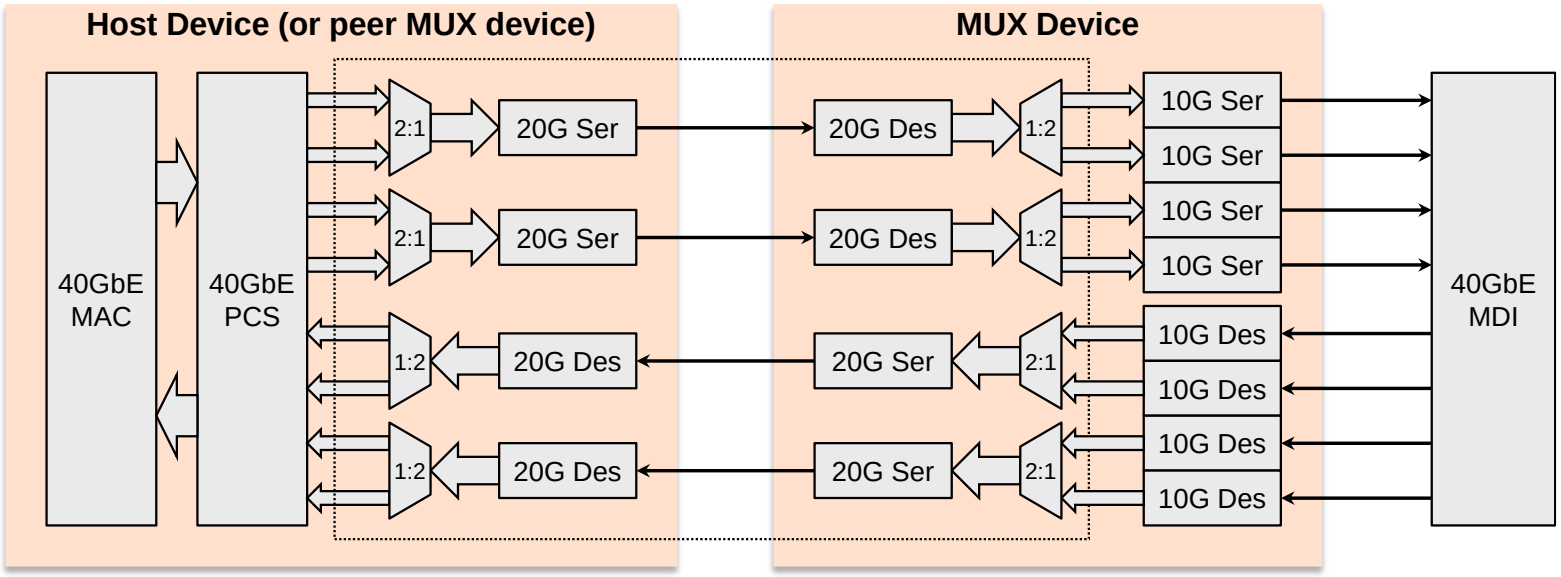
FEATURES

- Supports up to five bi-directional channels of the 2:1 Serial Multiplexing/Demultiplexing function
- Optional Redundant Link Mode feature (contact factory)
- IEEE and OIF 10, 25, 40, and 100G electrical standards
- Self adapting equalizer - eye opening capability
- Transmitter and TX pre-emphasis
- Per lane PRBS generator and bit error rate checker
- Reverse polarity control on all inputs and outputs
- Monitor and reference clock support
- Base register configuration and FW provided for ease of use
- Pin compatible with MSH320 Gearbox and MSH225 Retimer 17x17mm FCBGA package



MSH420 APPLICATION EXAMPLE

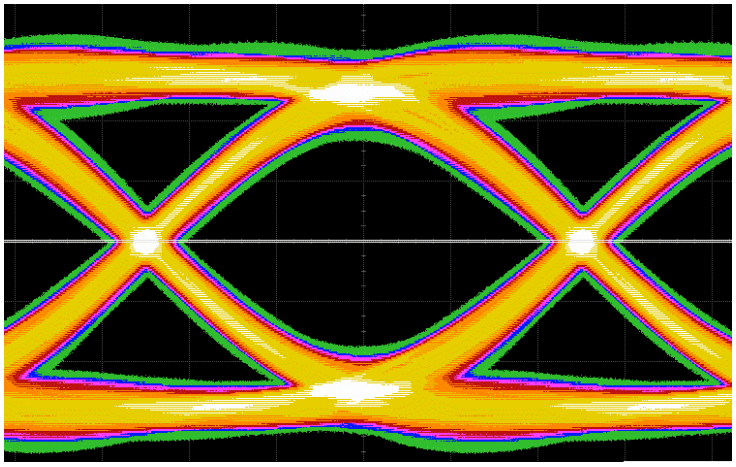
The MSH420 Mux/Demux device can be used to aggregate the four 10.3125 Gb/s lanes of a traditional 40Gb Ethernet link onto two 20.625 Gb/s lanes. This feature can be used to either halve the number or required physical lanes or double the throughput over the same number lanes.



MSH420 DEVICE SIGNAL INTEGRITY

To ensure signal integrity for 10G and 25G interfaces, the MSH420 has the following circuits:

- Opening the eye: A combined analog and digital RX equalizer
- Retiming: A data slicer plus a clock and data recovery circuit
- Bit stream alignment: Deserializer, frame sync and deskew functions
- Clock synchronization: An elastic buffer for data alignment
- Pre-distortion compensation: A serializer and transmit equalization circuit



PACKAGING

- 17mm x 17mm 256 FCBGA (1.0mm)

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For more information
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